EE310 – Chapter 4

MOS Field Effect Transistor

Lecture Slides

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Chap. 4 MOS Field Effect Transistor

MOSFET relative to BJT

- MOSFET can be made Very Small, and manufacturing is simpler
- MOSFET circuits take little power (CMOS)
- Both digital and analog functions possible
- 200M – 1B MOSFET's in VLSI

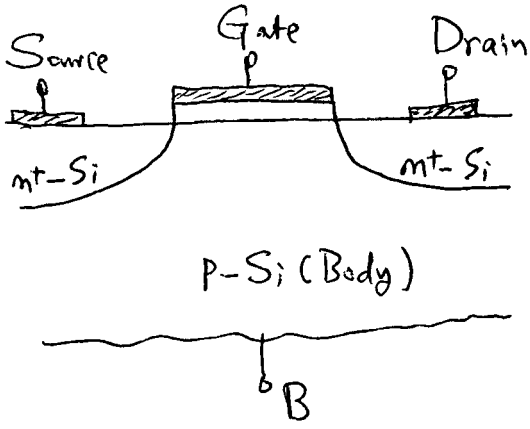
Goals of Chap. 4

- Familiarity with physical structure and Operation
- Terminal Characteristics, and Circuit Models
- Basic Amp Circuits (and Inverter if time allows)

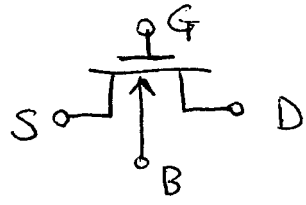
4.1 Physical Structure & Operation

(1) Device Structure

Fig.1



NMOS = N-channel MOSFET



- Gate oxide = insulator $\therefore$ I_G = DC Gate current = 0
  V_G affects conduction in Si
- Gate metal can be Aluminum or n+-Si (polycrystal)
  or p+-Si (")
- Device Size : L = Length of Channel 0.1 – 3 um
  W = Width of channel 0.2 – 100 um
- PN junctions S – B , D – B are reverse biased or zero biased.
  (n) (p) (n) (p)
  → often S – B is shorted and D-B is reverse b.
  $\therefore$ S – B – D is cutoff.
  → $V_S = V_B$ make MOSFET a 3-terminal device.
- V_G controls current between S and D

(3) Apply V_G to create Inversion Channel

Fig. 2

Key concepts:

- Channel = inversion layer @ Si surface that conducts current between S and D
- NMOS = n-channel MOSFET
  PMOS = p-channel MOSFET
- V_t = Threshold Voltage = V_{GS} just enough to create inversion channel

  ex) n-channel forms if $V_{GS} \geq V_t$ (NMOS)

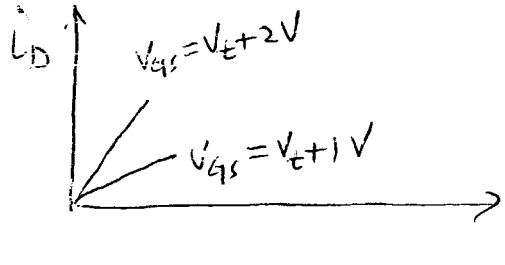
  p-channel forms if $V_{GS} \leq V_t$ (PMOS)

(4) V_{DS} = small

Fig. 3 – Fig. 4

NMOS

With the n-channel induced ($V_{GS} > V_t$), there is continuous channel between S and D. Channel acts as a conductor (or resistor)



applet

-4.4

4.1 From the description above of the operation of the MOSFET for small v_{DS}, we note that i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Find the constant of proportionality for the particular device whose characteristics are depicted in Fig. 4.4. Also, give the range of drain-to-source resistances corresponding to an overdrive voltage, $v_{GS} - V_t$, of 0.5 V to 2 V.

Ans. 1 mA/V^2; 2 kΩ to 0.5 kΩ

Let $i_D = B(V_{GS} - V_t)V_{DS}$. ① $B = (\quad)$

② $r_{DS}^{-1} = \frac{\partial i_D}{\partial V_{DS}} = B(V_{GS} - V_t) = (\quad)$ for $V_{GS} - V_t = 0.5V \leftrightarrow 2V$

Sol) ① Take the $V_{GS} = V_t + 1V$ data in Fig. 4

V_{DS} =	100 mV	200 mV
i_D =	0.1 mA	0.2 mA

$$B = \frac{\Delta i_D}{(V_{GS} - V_t)\Delta V_{DS}} = \frac{(0.2 - 0.1)\text{mA}}{1V \cdot (0.2 - 0.1)V} = 1\frac{\text{mA}}{V^2}$$

② $$r_{DS} = \frac{1}{B(V_{GS} - V_t)} = \begin{cases} \frac{1}{1\frac{\text{mA}}{V^2} \cdot 0.5V} = 2k\Omega \\ \frac{1}{1\frac{\text{mA}}{V^2} \cdot 2V} = 0.5k\Omega \end{cases}$$

(5) When V_{DS} is Large

Fig.5 Applet

As the Drain-end of Channel becomes 'pinched' because V_{DS} increases, the $i_D - V_{DS}$ curve 'bends' (and I-V becomes 'nonlinear') and eventually, i_D reaches a maximum, saturation value.

Fig.6

The maximum, saturation value of i_D happens when V_{DS} reaches $V_{GS} - V_t$ and the Drain-end of channel is pinched off.

Operating Modes

NMOS

(i) Triode (Linear) : $V_{GS} > V_t$ (Channel ON), $V_{DS} < V_{GS} - V_t$

(ii) Saturation : $V_{GS} > V_t$, $V_{DS} \geq V_{GS} - V_t$

(iii) Cutoff : $V_{GS} < V_t$

(6) Derivation of $i_D - V_{DS}$

Fig. 8

Consider the gate oxide 'stripe' of size Wdx.

- $(Wdx)C_{ox}$ = Capacitance of the 'stripe'
- dq = charge in channel under the 'stripe'
- $(V_{GS}-V_t)-V$ = voltage drop across oxide

where, $\begin{cases} V_{GS}-V_t = \text{'net' Gate Voltage} \\ V = \text{voltage in channel} \end{cases}$

$\therefore\ dq = (WdxC_{ox})(V_{GS}-V_t-V)$ from $Q=CV$

Current thru channel: $i = \frac{dq}{dt} = C_{ox}W(V_{GS}-V_t-V)\frac{dx}{dt}$

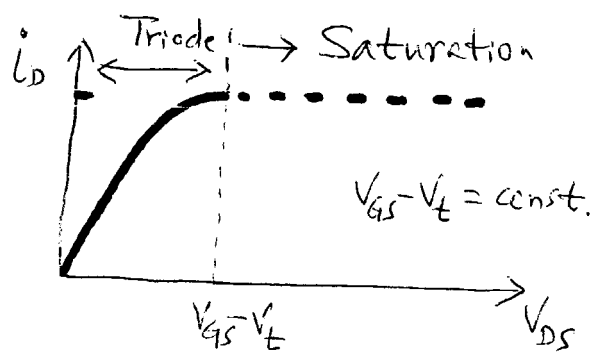
Carrier Velocity $= \frac{dx}{dt} = \mu_n E = -\mu_n \frac{dV}{dx}$

$\therefore\ i = -\mu_n C_{ox} W (V_{GS}-V_t-V)\frac{dV}{dx}$ Let $i_D = -i$

$$\Rightarrow \int_0^L i_D\,dx = \mu_n C_{ox} W \int_0^{V_{DS}} (V_{GS}-V_t-V)\,dV = \mu_n C_{ox} W \left[(V_{GS}-V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$$

$$\Rightarrow i_D = (\mu_n C_{ox})\frac{W}{L}\left[(V_{GS}-V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2\right]$$

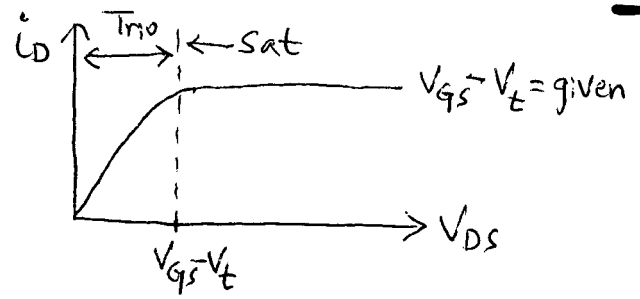
material property ↑ device size ↑ bias



$\Rightarrow$ Saturation i_D

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$$

$i_D - V_{DS}$ Summary



• Saturation:

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS}-V_t)^2 \quad \text{or} \quad \frac{1}{2} k_n V_{GST}^2$$

• Triode:

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad \text{or} \quad k_n\left[V_{GST}V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

where $k_n' \equiv \mu_n C_{ox}$ = process transconductance $\left[\frac{A}{V^2}\right]$

$k_n \equiv k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$ = Device transcond.

V_{ov} or $V_{GST} \equiv V_{GS} - V_t$ = Gate-to-S overdrive volt.

Note $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ = oxide capacitance/unit area

L, W ex) In 2003, $L_{min} = 0.13\,\mu m$

$W_{min} = 0.16\,\mu m$

ex) $L_{min} = 1.5\,\mu m$ $t_{ox} = 25\,nm$

$L_{min} = 0.13\,\mu m$ $t_{ox} = 2\,nm$

4.2 For a 0.8-μm process technology for which t_{ox} = 15 nm and μ_n = 550 cm^2/V·s, find C_{ox}, k_n', and the overdrive voltage $V_{OV} \equiv V_{GS} - V_t$ required to operate a transistor having W/L = 20 in saturation with I_D = 0.2 mA. What is the minimum value of V_{DS} needed?

Ans. 2.3 fF/μm^2; 127 μA/V^2; 0.40 V; 0.40 V

① C_{ox} ② k_n' ③ V_{ov}, V_{GST} ④ V_{DS} for Sat.

Sol) ① $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_0}{t_{ox}} = \frac{3.9 \times 8.8\times10^{-12}\,F/m}{15\times10^{-3}\,\mu m} = 2.3\times10^{-15}\,F/\mu m^2$

② $k_n' = \mu_n C_{ox} = 550\,cm^2/V\cdot s \times 2.3\,fF/\mu m^2 = 550\times(10^4)^2 \times 2.3\times10^{-15}\,\frac{F}{V\cdot s}$

$= 1.27\times10^{-4}\,A/V^2$

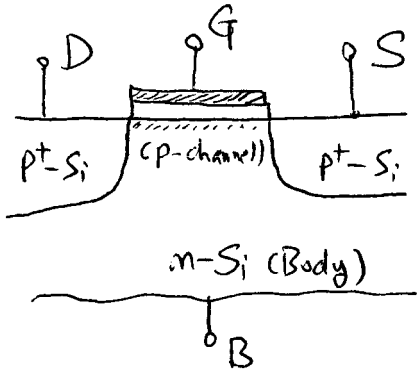
③ Sat: $I_D = \frac{1}{2}k_n'\frac{W}{L}V_{GST}^2$

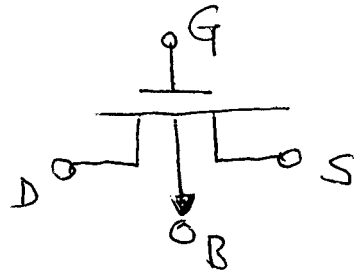
$\therefore V_{GST} = \sqrt{\frac{2I_D}{k_n'(W/L)}} = \sqrt{\frac{2\times0.2\times10^{-3}\,A}{1.27\times10^{-4}\frac{A}{V^2}\cdot 20}} = 0.4\,V$

④ SAT: $V_{DS} \geq V_{GST}$

$\therefore V_{DS} = 0.4\,V$ min.

(7) PMOS or P-channel MOSFET





- P-channel forms ib $\underline{V_{GS} < V_t}$
- i_D saturates and P-channel pinches off at D-end ib $\underline{V_{DS} \leq V_{GS} - V_t}$

(8) CMOS or Complementary MOS

Fig. 9

NMOS and pMOS on the same Silicon

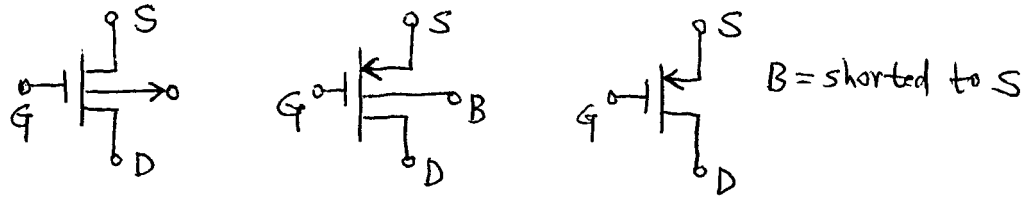
(9) Subthreshold region

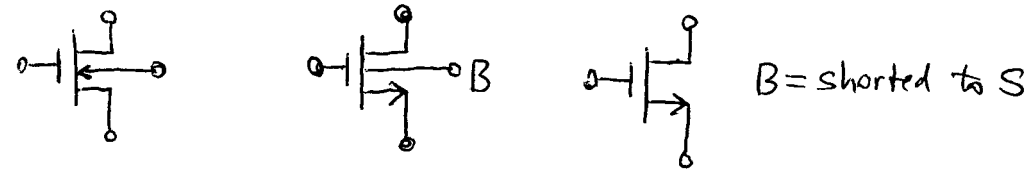
For NMOS with $V_{GS} < V_t$, no channel is present and $i_D \approx 0$ for any V_{DS}.

However, very small i_D is still present with $i_D \sim e^{bV_{GS}}$
This is called Subthreshold current, and
is increasingly important in modern deep submicron VLSI.

4.2 I-V Characteristics

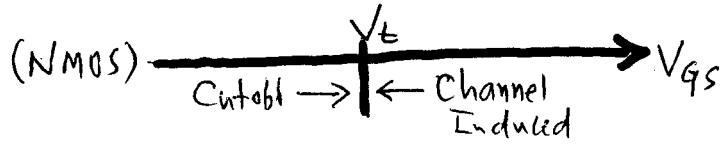
(1) Circuit Symbols

PMOS = 

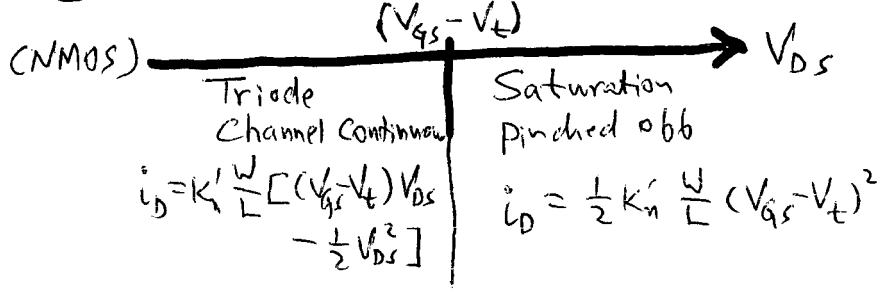
NMOS = 

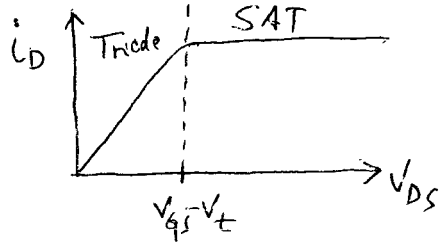
(2) $i_D - V_{DS}$ Characteristics, NMOS

i) Channel is Induced or Off : V_{GS}

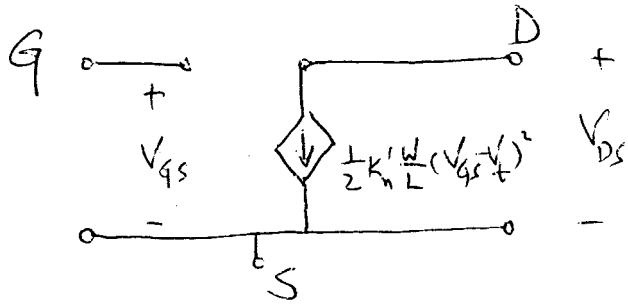


ii) Saturation mode or Triode mode : V_{DS}





SAT model



4.4 An enhancement-type NMOS transistor with $V_t = 0.7$ V has its source terminal grounded and a 1.5-V dc applied to the gate. In what region does the device operate for (a) $V_D = +0.5$ V? (b) $V_D = 0.9$ V? (c) $V_D = 3$ V?

Ans. (a) Triode; (b) Saturation; (c) Saturation

Enhancement NMOS : $V_t = 0.7V$ Note Enhancement means $V_t > 0$

$V_S = 0$ $V_G = 1.5$ (a) $V_D = 0.5$ (b) $V_D = 0.9$ (c) $V_D = 3$

Sol) $V_{GS} = 1.5 - 0 = 1.5V > V_t = 0.7$ ∴ Channel = induced

(a) $V_{DS} = 0.5$ $V_{GSt} = V_{GS} - V_t = 1.5 - 0.7 = 0.8$ ∴ Triode

(b) $V_{DS} = 0.9$ ∴ SAT

(c) $V_{DS} = 3$ ∴ SAT

4.5 If the NMOS device in Exercise 4.4 has $\mu_n C_{ox} = 100\ \mu A/V^2$, $W = 10\ \mu m$, and $L = 1\ \mu m$, find the value of drain current that results in each of the three cases (a), (b), and (c) specified in Exercise 4.4.

Ans. (a) 275 μA; (b) 320 μA; (c) 320 μA

Same NMOS as above. $K_n' = \mu_n C_{ox} = 100 \mu A/V^2$, $\frac{W}{L} = \frac{10}{1} = 10$

Sol)

(a) $V_{DS} = 0.5V$ Triode

$$i_D = K_n' \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] = 100 \frac{\mu A}{V^2} \cdot 10 \cdot \left[(1.5 - 0.7) \cdot 0.5 - \frac{0.5^2}{2} \right] V$$

$$= 275 \mu A$$

(b) $V_{DS} = 0.9V$ SAT

$$i_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} \cdot 100 \frac{\mu A}{V^2} \cdot 10 \cdot (1.5 - 0.7)^2 V^2$$

$$= 320 \mu A$$

(c) $V_{DS} = 3V$ SAT

$i_D = 320 \mu A$

4.6 An enhancement-type NMOS transistor with $V_t = 0.7$ V conducts a current $i_D = 100\ \mu$A when $v_{GS} = v_{DS} = 1.2$ V. Find the value of i_D for $v_{GS} = 1.5$ V and $v_{DS} = 3$ V. Also, calculate the value of the drain-to-source resistance r_{DS} for small v_{DS} and $v_{GS} = 3.2$ V.

Ans. 256 μA; 500 Ω

$i_D = 100\mu A$ @ $V_{DS} = V_{GS} = 1.2V$ for Enhancement NMOS $V_t = 0.7V$

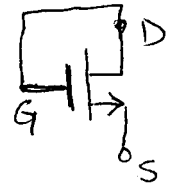
① $i_D = (\quad)$ @ $V_{GS} = 1.5V$, $V_{DS} = 3V$ Note Enhancement pMOS?

② $r_{DS} = (\quad)$ @ $V_{GS} = 3.2V$, small V_{DS}

Sol) operating mode?

$V_{GS} = 1.2V > V_t$ ∴ Channel Induced

$V_{DS} = V_{GS} > V_{GS} - V_t$ ∴ Saturation Note



Always SAT for Enhance. NMOS ∵ $V_{DS} = V_{GS} > V_{GS} - V_t$

SAT: $i_D = 100\mu A = \frac{1}{2} K_n (V_{GS} - V_t)^2 = \frac{1}{2} K_n (1.2 - 0.7)^2$

$\therefore K_n = \frac{2 \times 100mA}{(1.2-0.7)^2 V^2} = 800\ \mu A/V^2$

① $V_{DS} = 3V > V_{GSt}$ ∴ $i_D = \frac{1}{2} K_n V_{GSt}^2 = \frac{1}{2} \cdot 800\mu A/V^2 \cdot (1.5 - 0.7)^2 V^2 = 256\ \mu A$

② Small V_{DS} ∴ Triode $r_{DS} = \left(\frac{\Delta i_D}{\Delta V_{DS}}\right)^{-1} = (K_n V_{GSt})^{-1} = \left[800 \frac{\mu A}{V^2} \cdot 2.5V\right]^{-1} = 500\ \Omega$

4.7 An NMOS transistor is fabricated in a 0.4-μm process having $\mu_n C_{ox} = 200\ \mu$A/V^2 and $V_A' = 50$ V/μm of channel length. If $L = 0.8\ \mu$m and $W = 16\ \mu$m, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage $V_{OV} = 0.5$ V and $V_{DS} = 1$ V. Also, find the value of r_o at this operating point. If V_{DS} is increased by 2 V, what is the corresponding change in I_D?

Ans. 40 V; 0.025 V^{-1}; 0.51 mA; 80 kΩ; 0.025 mA

NMOS: $k_n' = \mu_n C_{ox} = 200 \frac{\mu A}{V^2}$, $V_A' = \frac{1}{\lambda'} = 50 \frac{V}{\mu m}$, $L = 0.8\mu m$, $W = 16\mu m$

① $V_A = \frac{1}{\lambda} = (\quad)V$ ② $i_D = (\quad)$ for $V_{ov} = V_{GSt} = 0.5V$, $V_{DS} = 1V$

③ $r_o = \frac{V_A}{I_D} = (\quad)$ ④ $\Delta i_D = (\quad)$ for $\Delta V_{DS} = 2V$

Sol) ① $V_A = L V_A' = 0.8\mu m \cdot 50 \frac{V}{\mu m} = 40V$, $\lambda = \frac{1}{V_A} = \frac{1}{40} V^{-1}$

② SAT: $i_D = \frac{1}{2} k_n' \frac{W}{L} V_{GSt}^2 \left(1 + \frac{V_{DS}}{V_A}\right) = \frac{1}{2} \cdot 200 \frac{\mu A}{V^2} \cdot \frac{16}{0.8} \cdot 0.5^2 V^2 \left(1 + \frac{1V}{40V}\right)$

$= 500\mu A\,(1 + 0.025) = 512.5\ \mu A$

③ $r_o = \frac{V_A}{I_D} = \frac{40V}{500\mu A} = 80\,k\Omega$ ④ $i_D = \frac{1}{2} k_n V_{GSt}^2 \left(1 + \frac{V_{DS}}{V_A}\right) = I_D \left(1 + \frac{V_{DS}}{V_A}\right)$

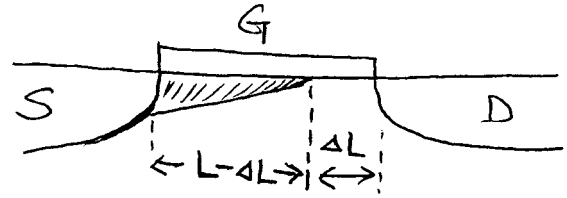
$\Delta i_D = I_D \frac{\Delta V_{DS}}{V_A} = 500\mu A \cdot \frac{2V}{40V} = 25\ \mu A$

(3) Transistor Output Resistance in SAT

r_o – due to Channel Length modulation by V_{DS}

Beyond Pinchoff (after Edge of Saturation)

Fig.15



$$i_D = \frac{1}{2}K_n' \frac{W}{L-\Delta L}(V_{GS}-V_t)^2 \simeq \frac{1}{2}K_n' \frac{W}{L}(V_{GS}-V_t)^2\left(1+\frac{\Delta L}{L}\right)$$

$$\boxed{i_D = \frac{1}{2}K_n' \frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}$$

Let $\Delta L \equiv \lambda' V_{DS}$

Define

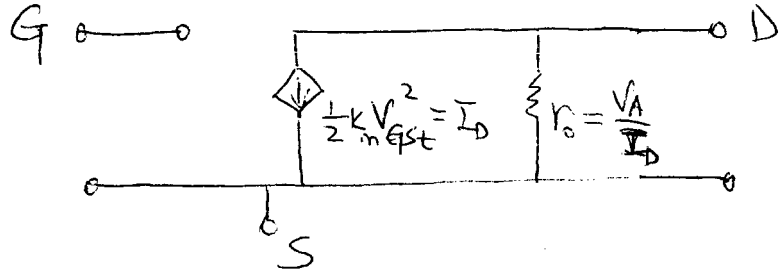
- $V_A' \equiv \frac{1}{\lambda'}$
- $\lambda \equiv \frac{\lambda'}{L}$
- $V_A \equiv \frac{1}{\lambda} = \frac{L}{\lambda'} = L V_A'$

Fig.16

Large-Signal model for SAT mode

$$i_D = \frac{1}{2}K_n V_{GSt}^2\left(1+\frac{V_{DS}}{V_A}\right) = I_D\left(1+\frac{V_{DS}}{V_A}\right)$$

Output resistance $r_o \equiv \left(\frac{\Delta i_D}{\Delta V_{DS}}\right)^{-1} = \frac{V_A}{I_D}$



4.8 The PMOS transistor shown in Fig. E4.8 has $V_t = -1$ V, $k_p' = 60\ \mu A/V^2$, and $W/L = 10$. (a) Find the range of V_G for which the transistor conducts. (b) In terms of V_G, find the range of V_D for which the transistor operates in the triode region. (c) In terms of V_G, find the range of V_D for which the transistor operates in saturation. (d) Neglecting channel-length modulation (i.e., assuming $\lambda = 0$), find the values of $|V_{OV}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75\ \mu A$. (e) If $\lambda = -0.02\ V^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in (d). (f) For $\lambda = -0.02\ V^{-1}$ and for the value of V_{OV} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

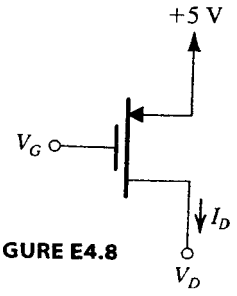


FIGURE E4.8

Ans. (a) $V_G \le +4$ V; (b) $V_D \ge V_G + 1$; (c) $V_D \le V_G + 1$; (d) 0.5 V, 3.5 V, ≤4.5 V; (e) 0.67 MΩ; (f) 78 μA, 82.5 μA, 0.67 MΩ (same).

PMOS Question!

$V_t = -1V$, $K_p' = \mu_p C_{ox} = 60 \frac{\mu A}{V^2}$ $\frac{W}{L} = 10$

(a) V_G range = ( ) for Induced channel, (b) V_D range = ( ) for Triode

(c) V_D range = ( ) for SAT, (d) $|V_{ov}| = |V_{GSt}| =$ ( ), $V_G =$ ( ), $V_D =$ ( )

(e) $\lambda = \frac{1}{V_A} = -0.02V^{-1}$, $r_o =$ ( ) for pmos in SAT with $I_D = 75\mu A$. Ignore V_A.

(f) $\lambda = -0.02V^{-1}$, $I_D =$ ( ) @ $V_D = 3V$, 0V @ $|V_{GSt}|$ from (d). Apparant $r_o =$ ( )

Sol) (a) $V_{GS} = V_G - 5 \le V_t = -1$ $\therefore V_G \le 5 - 1 = 4$ then PMOS conducts.

(b) Triode: $V_{DS} \ge V_{GS} - V_t$ (V_{DS} is less negative)

$V_D - 5 \ge V_G - 5 - (-1)$ $\therefore V_D \ge V_G + 1$ Triode

(c) SAT: $V_{DS} \le V_{GS} - V_t$ (V_{DS} is more negative)

$\therefore V_D \le V_G + 1$ SAT

(d) Neglect V_A: $I_d = 75\mu A = \frac{1}{2} K_p' \frac{W}{L} V_{GSt}^2 = \frac{1}{2} \cdot 60 \frac{\mu A}{V^2} \cdot 10 \cdot V_{GSt}^2$

$\therefore V_{GSt} = \pm\sqrt{\frac{75\mu A}{300\mu A/V^2}} = \pm 0.5V$ $\therefore V_{GSt} = -0.5V = V_{ov}$

(e) $V_A = \frac{1}{\lambda} = -\frac{1}{0.02} V = -50V$ $r_o = \frac{|V_A|}{I_d} = \frac{50V}{75\mu A} = 0.67M\Omega$

(f) $V_A = \frac{1}{\lambda} = -50V$. ① $V_{DS} = 3 - 5 = -2 < V_{GSt} = -0.5$ $\therefore$ SAT

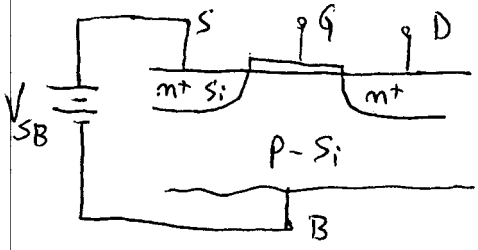
② $V_{DS} = 0 - 5 = -5 < V_{GSt}$ $\therefore$ SAT

$i_D = \frac{1}{2} K_p V_{GSt}^2 \left(1 + \frac{V_{DS}}{V_A}\right) = I_D \left(1 + \frac{V_{DS}}{V_A}\right) =$ ① $75\mu A \left(1 + \frac{-2}{-50}\right) = 78\mu A$

② $75\mu A \left(1 + \frac{-5}{-50}\right) = 82.5\mu A$

$r_o = \frac{\Delta V_{DS}}{\Delta i_D} = \frac{5 - 2\ V}{82.5 - 78\mu A} = 0.67M\Omega$

(5) The Body Effect - What happens when $V_B \neq V_S$?



Instead of shorting B to S,
Apply a reverse bias V_{SB}.

Effect: $V_t \uparrow$

$$\boxed{V_t = V_{to} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]}$$

where, γ = Body effect param $\equiv \dfrac{\sqrt{2q N_A \varepsilon_s}}{C_{ox}}$

$2\phi_f$ = physical param, 0.6 V typical

4.9 An NMOS transistor has $V_{t0} = 0.8$ V, $2\phi_f = 0.7$ V, and $\gamma = 0.4\ V^{1/2}$. Find V_t when $V_{SB} = 3$ V.
Ans. 1.23 V

sol) $V_t = V_{to} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$

$= 0.8V + 0.4V^{1/2}(\sqrt{0.7+3} - \sqrt{0.7})V^{1/2} = 0.8 + 0.435 = 1.23\ V$

(6) Temperature Effect

As Temp. ↑, k' ↓ and V_t ↓ $\left(\dfrac{dV_t}{dT} = -\dfrac{2mV}{^\circ C}\right)$
(dominant)

$\therefore I_d = \frac{1}{2} k' \frac{W}{L}(V_{GS} - V_t)^2$ ↓

(7) Breakdown

i) Drain-Body pn junction breaks down around 20-150 V
(soft avalanche)

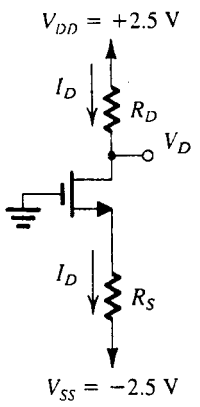
ii) Punch-~~Through~~; The pinchoff point moves all the way to S
The depletion (around D) extends all the way to S
→ happens around 20 V (no perma damage)
→ especially in modern Short channel device

iii) Gate Oxide Breakdown
happens around $V_{GS} \doteq 30$ V. Because C_G = small,
$V_G \sim \dfrac{Q_G}{C_G}$ can rise for even small Q_G.
→ prevent accumulating Q_G!
→ Input protection device (clamping diodes)

4.3 MOSFET Circuit at DC - Examples

D4.10 Redesign the circuit of Fig. 4.20 for the following case: $V_{DD} = -V_{SS} = 2.5$ V, $V_t = 1$ V, $\mu_n C_{ox} = 60\ \mu$A/V^2, $W/L = 120\ \mu$m/$3\ \mu$m, $I_D = 0.3$ mA, and $V_D = +0.4$ V.

Ans. $R_S = 3.3\ \text{k}\Omega$; $R_D = 7\ \text{k}\Omega$



Design for $I_D = 0.3$mA, $V_D = 0.4$V ① $R_S = (\ )$ ② $R_D = (\ )$

Sol) $V_{DS} \geq V_{GS} > V_{GSt}$ ∴ SAT

① $I_D = 0.3\text{mA} = \frac{1}{2} K_n' \frac{W}{L} V_{GSt}^2 = \frac{1}{2} \times 60 \frac{\mu A}{V^2} \times 40 \times V_{GSt}^2$

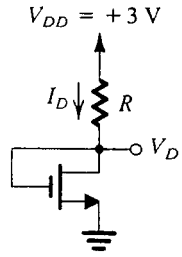
$\rightarrow V_{GSt} = \pm \sqrt{\frac{2 \times 300\mu A}{60 \times 40\ \mu A/V^2}} = \pm 0.5$ ∴ $V_{GSt} = 0.5 \rightarrow V_S = -1.5$V

$\rightarrow R_S = \frac{-1.5 - (-2.5)\text{V}}{0.3\text{mA}} = 3.3\text{k}\Omega$

② $R_D = \frac{2.5 - 0.4\text{V}}{0.3\text{mA}} = 7\text{k}\Omega$

Example 4.3 - Diode Connected MOSFET

Design the circuit in Fig. 4.21 to obtain a current I_D of 80 μA. Find the value required for R, and find the dc voltage V_D. Let the NMOS transistor have $V_t = 0.6$ V, $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$, $L = 0.8\ \mu$m, and $W = 4\ \mu$m. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



Design for $I_D = 80\mu$A ① $R = (\ )$ ② $V_D = (\ )$

Sol) $V_{DS} = V_{GS} > V_{GS} - V_t$ ∴ SAT

$I_D = 80\mu\text{A} = \frac{1}{2} K_n' \frac{W}{L} V_{GSt}^2 = \frac{1}{2} \cdot 200 \frac{\mu A}{V^2} \cdot 5 \cdot V_{GSt}^2$

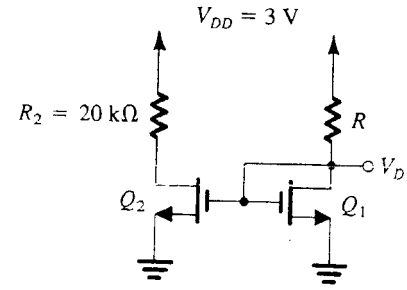
∴ $V_{GSt} = \pm \sqrt{\frac{2 \times 80\mu A}{200 \times 5\ \mu A/V^2}} = \pm 0.4$V ∴ $V_{GSt} = +0.4$V

$V_G - 0 - 0.6 = +0.4$

∴ $V_G = 1\text{V} = V_D$ ②

① $R = \frac{V_{DD} - V_D}{I_D} = \frac{3 - 1}{0.08\text{mA}} = 25\text{k}\Omega$

4.12 Consider the circuit of Fig. 4.21, which is designed in Example 4.3 (to which you should refer before solving this problem). Let the voltage V_D be applied to the gate of another transistor Q_2, as shown in Fig. E4.12. Assume that Q_2 is identical to Q_1. Find the drain current and voltage of Q_2. (Assume $\lambda = 0$.)



Ans. 80 μA; +1.4 V

Find ① $I_{D2} = (\ )$ ② $V_{D2} = (\ )$, Neglect λ

Sol) Q_1 and Q_2 have the same $V_{GSt} \rightarrow$ Same I_D

① $I_{D2} = I_{D1} = 80\mu$A from e 4.3 above

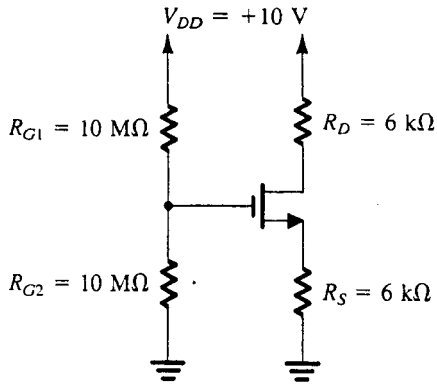
② $V_{D2} = V_{DD} - I_{D2} R_2 = 3 - 0.08\text{mA} \times 20\text{k}\Omega = 1.4$V

check SAT: $V_{DS2} = 1.4 > V_{GSt} = +0.4$V o/c

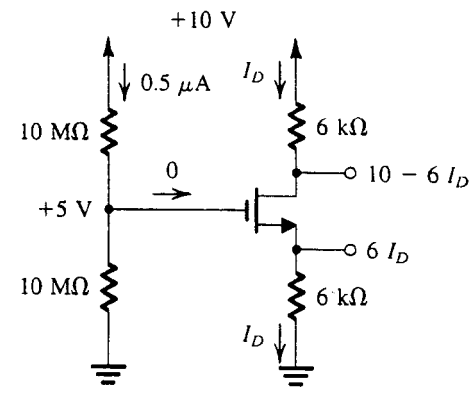
(Current Mirror)

Example 4.5

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).



(a)



(b)

Analyze for all V's and I's

Sol) $V_G = 5V$ $V_{GSt} = 4 - 6I_D$ $V_{DS} = 10 - 12I_D$

Assume SAT : $I_D = \frac{1}{2}K_n'\frac{W}{L}V_{GSt}^2 = \frac{1}{2}\cdot 1\frac{mA}{V^2}\cdot(4-6I_D)^2V^2$

$2I_D = (4-6I_D)^2$ $\therefore I_D = \frac{50 \pm 14}{2\times 36} = 0.89$ or 0.5 mA

$I_D = 0.89$mA $\rightarrow$ $V_{GSt} = 4 - 6\times 0.89 = -1.34$ NO!

$I_D = 0.5$mA $\rightarrow$ $V_{GSt} = 4 - 6\times 0.5 = 1V$ yes.

$V_G = 5V$ $V_S = 4 - 6\times 0.5 = 1V$ $V_D = 10 - 6\times 0.5 = 7V$

4.14 For the circuit of Fig. 4.23, what is the largest value that R_D can have while the transistor remains in the saturation mode?

Ans. 12 kΩ

Largest value of R_D that has NMOS still in SAT?

Sol) In Example 4.5

$V_{DS} = V_{DD} - R_D I_D - R_S I_D$

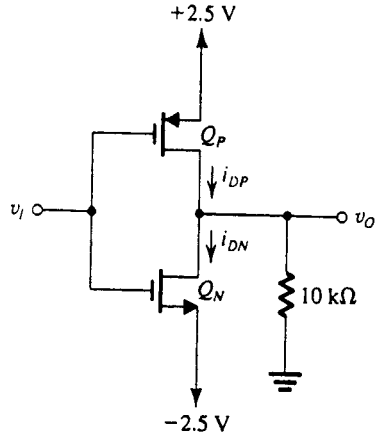
$= 10 - 0.5\times R_D - 0.5\times 6 = 7 - 0.5R_D$

$\geq V_{GSt} = 1V$ $\therefore R_D \leq \frac{7-1}{0.5} = 12k\Omega$

Max $R_D = 12k\Omega$

Example 4.7

The NMOS and PMOS transistors in the circuit of Fig. 4.25(a) are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1\ \text{V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0\ \text{V}$, $+2.5\ \text{V}$, and $-2.5\ \text{V}$.



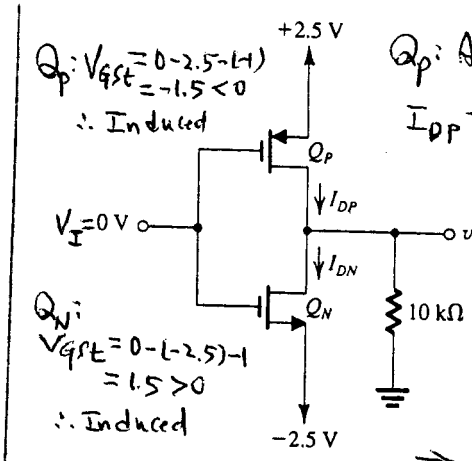
(a)

Q_P: $V_{GSt} = 0-2.5-(-1) = -1.5 < 0$

∴ Induced

Q_N: $V_{GSt} = 0-(-2.5)-1 = 1.5 > 0$

∴ Induced



(b)

Q_P: Assume SAT

$I_{DP} = \frac{1}{2} k_p V_{GSt}^2 = \frac{1}{2} \cdot 1 \cdot 1.5^2 = 1.125\ \text{mA}$

Q_N: Assume SAT

$I_{DN} = \frac{1}{2} K_n V_{GSt}^2 = \frac{1}{2} \times 1 \times 1.5^2 = 1.125\ \text{mA}$

$\Rightarrow V_o = 0$ From Symmetry.

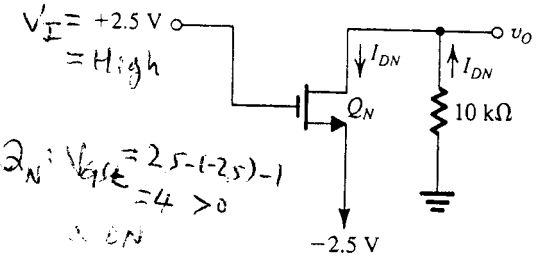
Q_P: $V_{GSt} = 2.5-2.5-(-1) = +1 > 0$

∴ OFF

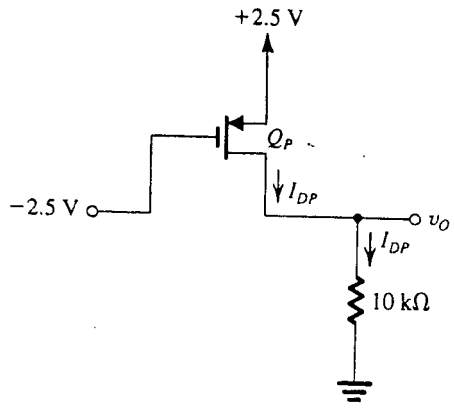
$V_I = +2.5\ \text{V} = \text{High}$

Q_N: $V_{GSt} = 2.5-(-2.5)-1 = 4 > 0$

∴ ON



(c)



(d)

If SAT, then

$I_{DN} = \frac{1}{2} K_n V_{GSt}^2 = \frac{1}{2} \times 1 \times 4^2 = 8\ \text{mA}$

$V_o = -8\ \text{mA} \times 10\ \text{k}\Omega = -8\ \text{V}$!

Assume Triode and Low V_{DS}:

$I_{DN} = K_n V_{GSt} V_{DS} = 1 \times 4 \times (V_o + 2.5)\ \text{mA}$

$= \frac{0 - V_o}{10\text{k}}$ $\quad \therefore V_o = \frac{10}{-41} = -2.44\ \text{V}$

Therefore,

$V_{DS} = V_o + 2.5 = 0.06\ \text{V}$ small

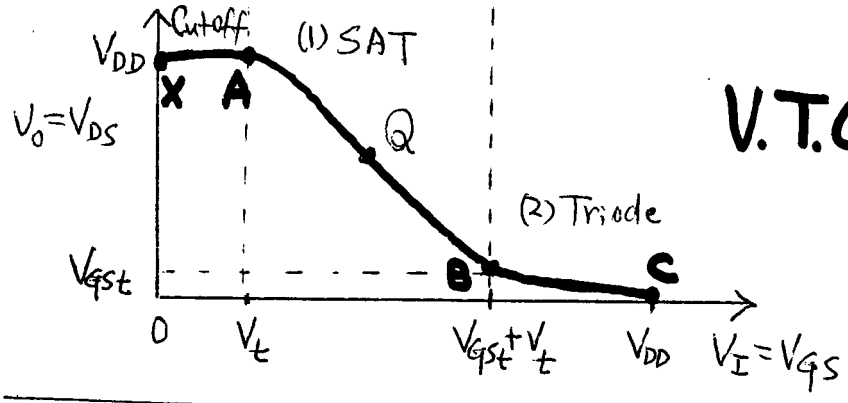
$I_{DN} = 1 \times 4 \times 0.06 = 0.244\ \text{mA}$

4.4 MOSFET as Amp or Switch

Fig.26

Common-Source Amp.

$V_O = V_{DD} - R_D i_D$



V.T.C.

(1) SAT

$$V_O = V_{DD} - R_D i_D = V_{DD} - R_D \tfrac{1}{2} K_n (V_I - V_t)^2$$

$$A_V = \left.\frac{\partial V_O}{\partial V_I}\right|_Q = \left. -R_D K_n (V_I - V_t)\right|_Q = -\frac{2(V_{DD}-V_O)}{V_{GST}} = -\frac{V_{RD}}{V_{GST}}$$

(2) Triode: $V_O = V_{DD} - R_D i_D = V_{DD} - R_D K_n [(V_I - V_t)V_O - \tfrac{1}{2}V_O^2]$

$$\approx V_{DD} - R_D K_n (V_I - V_t) V_O = V_{DD} - \frac{R_D}{r_{DS}} V_O = V_{DD} \frac{r_{DS}}{r_{DS}+R_D} \approx V_{DD} \frac{r_{DS}}{R_D}$$

Switch: XA $\longleftrightarrow$ C

(Low In, high Out) (high In, low Out)

Amplifier:
- MOS is biased at Q-point
  Small signal in.
- Design a good Q-pt:

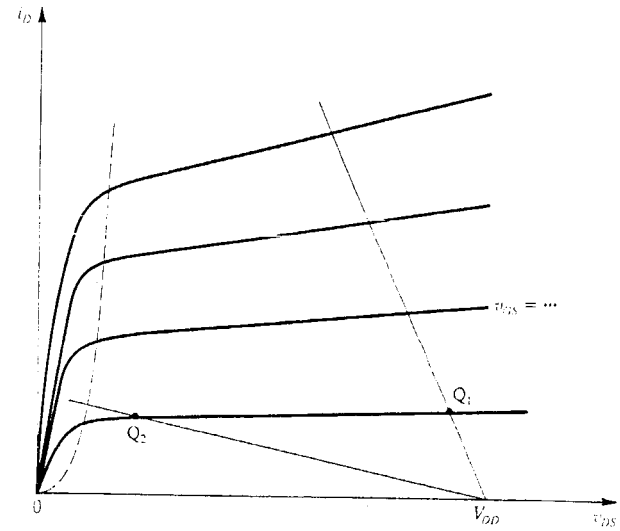


FIGURE 4.27

Example 4.8

Find values in VTC, (Fig. 2.6(b))
for $K_n = K_n' \frac{W}{L} = 1 \frac{mA}{V^2}$, $V_t = 1V$, $R_D = 18k\Omega$, $V_{DD} = 10V$

Sol)

(a) point X: $V_I = 0V$ $V_o = 10V$

(b) point A: $V_I = V_t = 1V$ $V_o = 10V$

(c) point B: $V_o = V_{GST}$ $V_I = V_{GS} = V_{GST} + V_t = V_o + V_t$

$$V_o = V_{DD} - R_D i_D = V_{DD} - R_D \frac{1}{2} K_n (V_I - V_t)^2 = V_{DD} - R_D \frac{1}{2} K_n V_o^2$$

$$= 10 - 18 \times \frac{1}{2} \times 1 \times V_o^2 = 10 - 9V_o^2 \quad \text{or} \quad 9V_o^2 + V_o - 10 = 0$$

$$\Rightarrow V_o = 1 \text{ or } -\cancel{\frac{10}{9}} \qquad (9V_o + 10)(V_o - 1) = 0$$

$$\therefore V_I = V_o + V_t = 1 + 1 = 2V \qquad V_o = 1V$$

(d) Point C: $V_I = V_{DD} = 10V$ $V_o \simeq V_{DD} \frac{r_{DS}}{R_D} = \frac{V_{DD}}{R_D} \frac{1}{K_n V_{GST}}$

$$= \frac{10V}{18k\Omega} \frac{1}{1 \frac{mA}{V^2} (10-1)V} = 0.06V$$

(e) Q-point and Voltage Gain

B (2, 1) —— A (1, 10)

Q-pt: $(V_I, V_o) = (2, 1)$

If Q-pt is chosen at $V_o = 4V$, then

$$V_{R_D} = V_{DD} - V_o = 10 - 4 = 6V$$

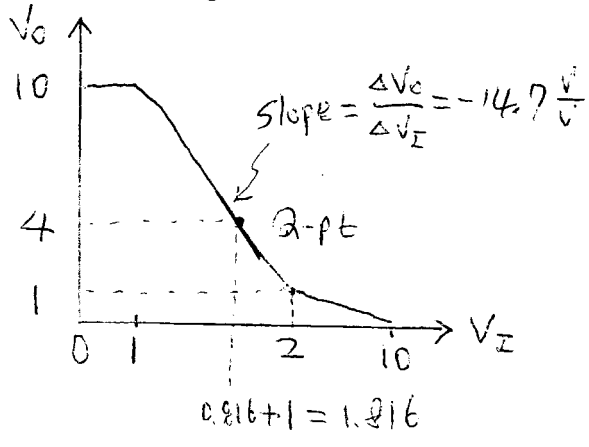
$$I_D = \frac{V_{R_D}}{R_D} = \frac{6V}{18k\Omega} = 0.333mA$$

$$= \frac{1}{2} \cdot 1 \frac{mA}{V^2} \cdot V_{GST}^2$$

$$\Rightarrow V_{GST} = \sqrt{2 \times 0.333} = 0.816V$$

to find $A_v = -\frac{2V_{R_D}}{V_{GST}}$

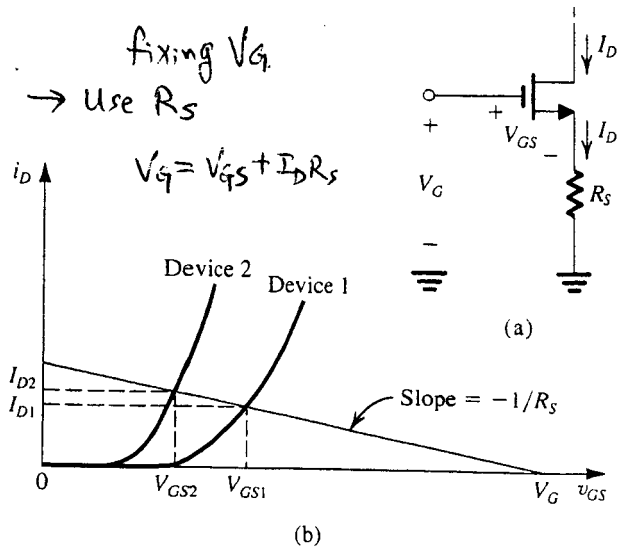
$$\therefore A_v = -\frac{2 \times 6V}{0.816V} = -14.7 \frac{V}{V}$$



4.5 Biasing MOS Amp Circuits

fixing V_G
→ use R_S

$V_G = V_{GS} + I_D R_S$



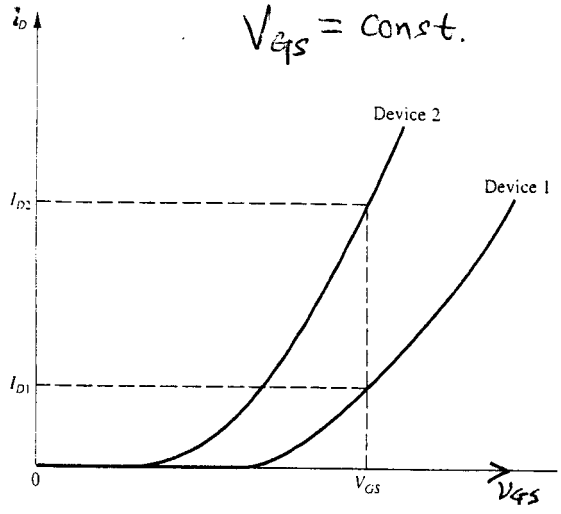


FIGURE 4.29

(1) Fix V_{GS}

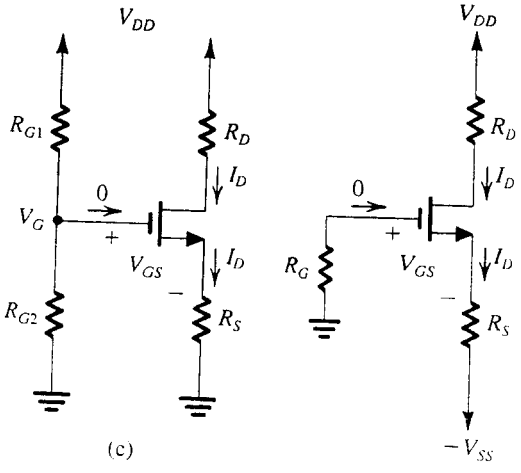
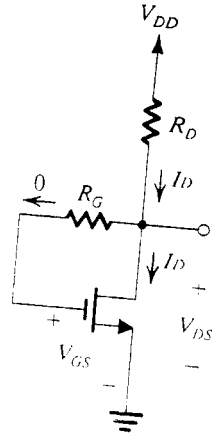


FIGURE 4.30

(2) Use D-to-G Feedback R_G



$V_{GS} = V_{DS} = V_{DD} - I_D R_D$

FIGURE 4.32
tance, R_G.

(3) Constant Current Source

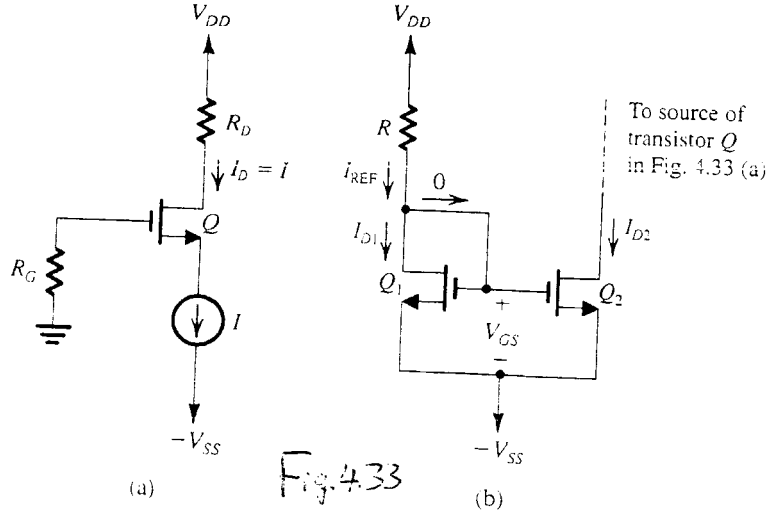


Fig. 4.33

$$I = I_{D2}$$

$$I_{D2} = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

D4.20 Design the circuit of Fig. 4.30(e) to operate at a dc drain current of 0.5 mA and $V_D = +2$ V. Let $V_t = 1$ V, $k_n'W/L = 1$ mA/V^2, $\lambda = 0$, $V_{DD} = V_{SS} = 5$ V. Use standard 5% resistor values (see Appendix G), and give the resulting values of I_D, V_D, and V_S.

Fig.30(e): $R_S = (\quad)$, $R_D = (\quad)$; $I_D = (\quad)$, $V_D = (\quad)$ $V_S = (\quad)$; 5% R in Appdx G

Sol) $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-2}{0.5} = 6\text{k}\Omega \rightarrow 6.2\text{k}\Omega$ (Appendix G: 5% R)

$I_D = \frac{1}{2}K_n V_{GSt}^2 = \frac{1}{2}\cdot 1 \cdot V_{GSt}^2 \Rightarrow V_{GSt} = 1\text{V} = V_G - V_S - V_t = 0 - V_S - 1 \therefore V_S = -2\text{V}$

$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-2-(-5)}{0.5} = 6\text{k}\Omega \rightarrow 6.2\text{k}\Omega$ (Appdx G)

If $R_S = R_D = 6.2\text{k}\Omega$, then I_D will be slightly different from 0.5mA:

$I_D = \frac{1}{2}K_n V_{GSt}^2 = \frac{1}{2}\cdot 1 \cdot (0 - V_S - 1)^2$ $\qquad V_S = -5\text{V} + 6.2\text{k}\Omega \cdot I_D$

$2I_D = (4 - 6.2I_D)^2 \Rightarrow I_D = 0.49\text{mA}$ or 0.896mA

$\downarrow V_{GS} = 1.962\text{V}$ $\qquad \downarrow V_{GS} = -0.322$

$\therefore I_D = 0.49\text{mA}$, $V_S = -1.962\text{V}$

$V_D = 5 - 6.2 \times 0.49 = 1.962\text{V}$

D4.21 It is required to design the circuit in Fig. 4.32 to operate at a dc drain current of 0.5 mA. Assume $V_{DD} = +5$ V, $k_n'W/L = 1$ mA/V^2, $V_t = 1$ V, and $\lambda = 0$. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

Fig.32: $R_D = (\quad)$; If 5% R, then $I_D = (\quad)$ $V_D = (\quad)$

Sol) $I_D = 0.5\text{mA} = \frac{1}{2}\cdot 1 \cdot V_{GSt}^2 \therefore V_{GSt} = 1\text{V} = V_G - 0 - 1 \Rightarrow V_G = 2\text{V} = V_D$ (why?)

$R_D = \frac{5-2}{0.5} = 6\text{k}\Omega \longrightarrow 6.2\text{k}\Omega$ (5%-R in Appdx G) $\longrightarrow I_D$ slightly from 0.5mA

$I_D = \frac{1}{2}\times 1 \times (V_G - 0 - 1)^2 = \frac{1}{2}(V_D - 1)^2 = \frac{1}{2}(V_{DD} - R_D I_D - 1)^2$

$\Rightarrow 2I_D = (4 - 6.2I_D)^2 \Rightarrow I_D = \frac{51.6 \pm 14.22}{76.88} = 0.486\text{mA}$ or 0.856mA

$\downarrow V_D = 1.987\text{V}$ $\qquad \downarrow V_D = -0.307\text{V}$

$\Rightarrow I_D = 0.486\text{mA}$, $V_D = 1.987\text{V}$

D4.22 Using two transistors Q_1 and Q_2 having equal lengths but widths related by $W_2/W_1 = 5$, design the circuit of Fig. 4.33(b) to obtain $I = 0.5$ mA. Let $V_{DD} = -V_{SS} = 5$ V, $k_n'(W/L)_1 = 0.8$ mA/V^2, $V_t = 1$ V, and $\lambda = 0$. Find the required value for R. What is the voltage at the gates of Q_1 and Q_2? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?

Fig.33: $R = (\quad)$ $V_{G1} = (\quad) = V_{G2}$, Lowest $V_{D2} = (\quad)$ for SAT?

Sol) $I_{D2} = I = 0.5\text{mA}$ $\qquad I_{D1} = I_{D2}\frac{(W/L)_1}{(W/L)_2} = 0.5\text{mA}\frac{1}{5} = 0.1\text{mA} = I_{REF}$

$I_{D1} = 0.1\text{mA} = \frac{1}{2}\cdot K_{n1}\cdot V_{GSt1}^2 = \frac{1}{2}\times 0.8\frac{\text{mA}}{\text{V}^2}\times V_{GSt1}^2 \Rightarrow V_{GSt1} = 0.5\text{V}$ $\quad V_{GS1} = 1 + 0.5 = 1.5$

$\Rightarrow V_{G1} = 1.5 - 5 = -3.5\text{V}$

$R = \frac{V_{DD} - V_{G1}}{I_{D1}} = \frac{5-(-3.5)}{0.1} = 85\text{k}\Omega$

For Q_2=SAT, $V_{DS2} \geq V_{GSt} = 0.5\text{V} \Rightarrow V_{D2} \geq V_{S2} + 0.5 = -4.5\text{V}$

minimum V_{D2} for SAT.

4.6 Small-Signal Models

(2) Total (DC+ac) Currents at Drain

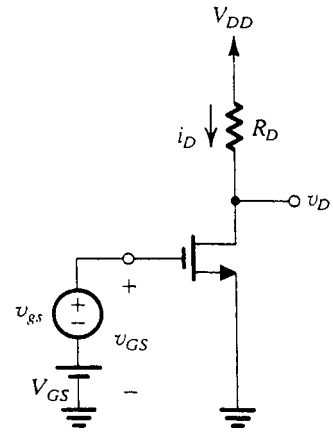


Fig. 4.34

$$\underbrace{v_{GS}}_{\text{tot}} = \underbrace{V_{GS}}_{\text{DC}} + \underbrace{v_{gs}}_{\text{ac}}$$

$$i_D = I_D + i_d = \frac{1}{2}k_n(V_{GS}+v_{gs}-V_t)^2$$

$$= \frac{1}{2}k_n(V_{GS}-V_t)^2 + k_n(V_{GS}-V_t)v_{gs} + \frac{1}{2}k_n v_{gs}^2$$

Ignored for $V_{GSt} \gg \frac{1}{2}v_{gs}$

$$\simeq \underbrace{\frac{1}{2}k_n V_{GSt}^2}_{(I_D)} + \underbrace{k_n V_{GSt} v_{gs}}_{(i_d)}$$

Small-Signal ($v_{gs} \ll 2V_{GSt}$)

$$i_d = k_n V_{GSt} v_{gs} \equiv g_m v_{gs}$$

Transconductance: $g_m = \frac{\partial i_d}{\partial v_{gs}} = k_n V_{GSt}$ or $k_n' \frac{W}{L}(V_{GS}-V_t)$

(3) Voltage Gain $A_v = \frac{v_d}{v_{gs}}$

From Fig. 34,

$$v_D = V_{DD} - i_D R_D = (V_{DD} - I_D R_D) - i_d R_D$$
$$= (DC) \qquad (ac)$$

Signal Drain voltage

$$v_d = -i_d R_D = -g_m v_{gs} R_D$$

$$\boxed{A_v = \frac{v_d}{v_{gs}} = -g_m R_D}$$

(5) Small-Signal Model: Hybrid-π model

(a) $i_d = g_m v_{gs}$ neglecting λ

(b) $i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$ including λ (or r_o)

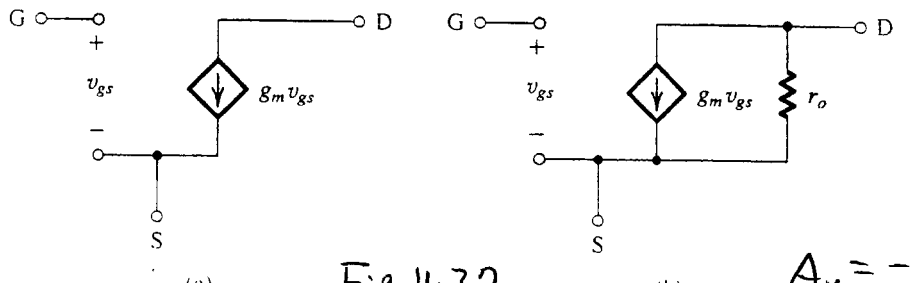


Fig. 4.37

$A_v = -g_m(R_D \| r_o)$

(6) Calculating g_m

$g_m = k_n V_{GSt}$ (if you know V_{GS})

$g_m = \sqrt{2 k_n I_D}$ (if you know I_D)

$g_m = \frac{2 I_D}{V_{GSt}}$

Note $I_D = \frac{1}{2} k_n V_{GSt}^2$

$\rightarrow 2 k_n I_D = (k_n V_{GSt})^2$

$\rightarrow \frac{2 I_D}{V_{GSt}} = k_n V_{GSt}$

Note Recall BJT: $g_m = \frac{I_C}{V_T}$

Discussion on g_m – MOSFET vs. BJT

MOSFET $g_m = \sqrt{2 k_n' \frac{W}{L} I_D}$, BJT $g_m = \frac{I_C}{V_T}$

ex) MOS: $I_D = 0.5mA$, $k_n' = 0.1 \frac{mA}{V^2}$

$\frac{W}{L} = 1 \Rightarrow g_m = \sqrt{2 \times 0.1 \times 1 \times 0.5} = 0.32 \frac{mA}{V}$

$\frac{W}{L} = 100 \Rightarrow g_m = \sqrt{2 \times 0.1 \times 100 \times 0.5} = 3.2 \frac{mA}{V}$

BJT: $I_C = 0.5mA$

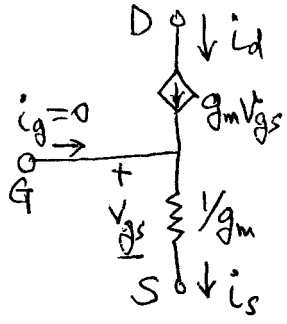
$g_m = \frac{0.5mA}{0.025V} = 20 \frac{mA}{V}$

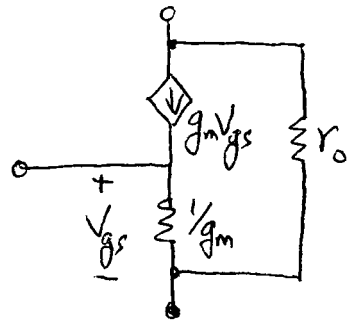
ex) MOS g_m – Design parameters are any Two of $\frac{W}{L}$, I_D, V_{GSt}

(7) Small-Signal Model: T-model

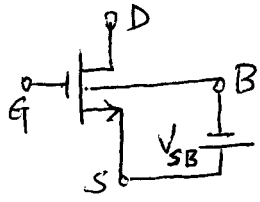
$i_d = g_m v_{gs} = i_s$

$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$ including r_o





(8) Including the Body-Effect



Recall $V_t = V_{to} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$

$= V_t(V_{SB})$

$\rightarrow i_D = \frac{1}{2} k_n \left[V_{GS} - V_t(V_{SB})\right]^2 \rightarrow i_D \downarrow$ as $V_t \uparrow$

Body-Effect Transconductance [for signal comp $i_d = g_{mb} v_{bs}$]

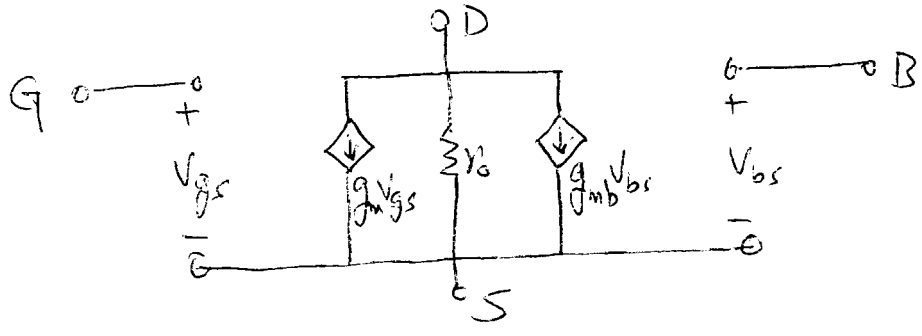
$$g_{mb} \equiv \frac{\partial i_D}{\partial V_{BS}} = k_n (V_{GS} - V_t)\left(-\frac{\partial V_t}{\partial V_{BS}}\right) \equiv k_n V_{GSt} \chi = \chi g_m$$

where, $\chi = -\frac{\partial V_t}{\partial V_{BS}} = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$

- Signal drain current i_d including r_o and body-effect

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} + g_{mb} v_{bs}$$

- π-model including r_o and Body-effect



4.24 An NMOS transistor has $\mu_n C_{ox} = 60\ \mu A/V^2$, $W/L = 40$, $V_t = 1$ V, and $V_A = 15$ V. Find g_m and r_o when (a) the bias voltage $V_{GS} = 1.5$ V, and when (b) the bias current $I_D = 0.5$ mA.

$g_m = (\quad)$, $r_o = (\quad)$ (a) $V_{GS} = 1.5V$ (b) $I_D = 0.5mA$

Sol) (a) $V_{GS} = 1.5V \rightarrow V_{GSt} = 1.5 - 1 = 0.5 \rightarrow g_m = k_n V_{GSt} = 60\frac{\mu A}{V^2} \times 40 \times 0.5 = 1200\frac{\mu A}{V}$

$\rightarrow I_D = \frac{1}{2} k_n V_{GSt}^2 = \frac{1}{2} \times 60\frac{\mu A}{V^2} \times (0.5V)^2 = 300\mu A \rightarrow r_o = \frac{V_A}{I_D} = \frac{15V}{0.3mA} = 50k\Omega$

(b) $I_D = 0.5mA \rightarrow g_m = \sqrt{2k_n I_D} = \sqrt{2 \times 0.06\frac{mA}{V^2} \times 40 \times 0.5mA} = 2.4\frac{mA}{V}$, $r_o = \frac{15V}{0.5mA} = 30k\Omega$

4.25 A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $k_n' = 50\ \mu A/V^2$, find the required W/L ratio and the overdrive voltage.

$\frac{W}{L} = (\quad)$, $V_{GSt} = (\quad)$ for $I_D = 0.1mA$, $g_m = 1\frac{mA}{V}$

Sol) $g_m = \sqrt{2k_n' \frac{W}{L} I_D} \rightarrow \frac{W}{L} = \frac{g_m^2}{2k_n' I_D} = \frac{(1mA/V)^2}{2 \times 0.05\frac{mA}{V^2} \times 0.1mA} = 100$

$g_m = \frac{2I_D}{V_{GSt}} \rightarrow V_{GSt} = \frac{2I_D}{g_m} = \frac{2 \times 0.1}{1} = 0.2V$

4.26 For a fabrication process for which $\mu_p = 0.4\mu_n$, find the ratio of the width of a PMOS transistor to the width of an NMOS transistor so that the two devices have equal g_m for the same bias conditions. The two devices have equal channel lengths.

PMOS vs. NMOS: $\mu_p = 0.4\mu_n$, $|V_{GSTp}| = |V_{GSTn}|$, $L_p = L_N$; $\frac{W_p}{W_N} = (\quad)$ for equal g_m

Sol) $g_{mp} = k_p'\left(\frac{W}{L}\right)_p V_{GSTp} = k_n'\left(\frac{W}{L}\right)_N V_{GSTN} = g_{mN}$

$\rightarrow k_p' W_p = k_n' W_N \rightarrow \frac{W_p}{W_N} = \frac{k_n'}{k_p'} = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{\mu_n}{0.4\mu_n} = 2.5$

4.27 For an NMOS transistor with $2\phi_f = 0.6$ V, $\gamma = 0.5\ V^{1/2}$, and $V_{SB} = 4$ V, find $\chi \equiv g_{mb}/g_m$.

Sol) $\chi = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} = \frac{0.5}{2\sqrt{0.6 + 4}} = 0.12$ or $g_{mb} = 0.12 g_m$

4.29 Use the formulas in Table 4.2 to derive an expression for $(g_m r_o)$ in terms of V_A and V_{OV}. As we shall see in Chapter 6, this is an important transistor parameter and is known as the intrinsic gain. Evaluate the value for $g_m r_o$ for an NMOS transistor fabricated in a 0.8-μm CMOS process for which $V_A' = 12.5\ V/\mu m$ of channel length. Let the device have minimum channel length and be operated at an overdrive voltage of 0.2 V.

$g_m r_o$ = Intrinsic Gain = $(\quad)$ for $V_A' = 12.5\frac{V}{\mu m}$, $L = 0.8\ \mu m$, $V_{GST} = 0.2V$

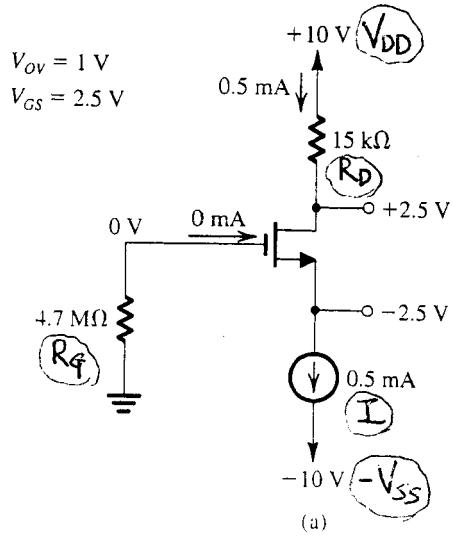
Sol) $g_m r_o = \left(\frac{2I_D}{V_{GST}}\right)\left(\frac{V_A}{I_D}\right) = \frac{2V_A}{V_{GST}} = \frac{2 \times 12.5\frac{V}{\mu m} \times 0.8\mu m}{0.2V} = 100\frac{V}{V}$

4.7 Single-Stage MOS Amplifiers

(1) Basic Structure and DC Bias

4.30 Consider the circuit of Fig. 4.42 for the case $V_{DD} = V_{SS} = 10$ V, $I = 0.5$ mA, $R_G = 4.7$ MΩ, $R_D = 15$ kΩ, $V_t = 1.5$ V, and $k_n'(W/L) = 1$ mA/V^2. Find V_{OV}, V_{GS}, V_G, V_S, and V_D. Also, calculate the values of g_m and r_o, assuming that $V_A = 75$ V. What is the maximum possible signal swing at the drain for which the MOSFET remains in saturation?

Ans. See Fig. E4.30; without taking into account the signal swing at the gate, the drain can swing to −1.5 V, a negative signal swing of 4 V.



$V_t = 1.5V$ $K_n = K_n' \frac{W}{L} = 1 \frac{mA}{V^2}$ Find: ① $V_{OV} = V_{GST}$
② V_{GS} ③ V_G ④ V_S ⑤ V_D ⑥ g_m ⑦ r_o for $V_A = 75V$
⑧ max $\hat{v}_o$ for Saturation

Sol)

① $V_{GST} = \sqrt{\frac{2I}{K_n}} = \sqrt{\frac{2 \times 0.5mA}{1 mA/V^2}} = 1V$

② $V_{GS} = V_{GST} + V_t = 1 + 1.5 = 2.5$

③ $V_G = 0$ ④ $V_S = V_G - V_{GS} = 0 - 2.5 = -2.5$

⑤ $V_D = V_{DD} - I_D R_D = 10 - 0.5m \times 15K = 2.5V$

⑥ $g_m = \sqrt{2K_n I_D} = \sqrt{2 \times 1 \times 0.5} = 1 \frac{mA}{V}$

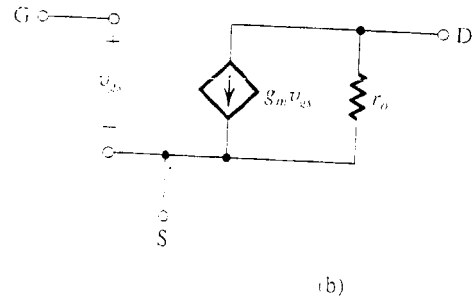
⑦ $r_o = \frac{V_A}{I_D} = \frac{75V}{0.5mA} = 150 K\Omega$

⑧ max $\hat{v}_o$ for MOS in SAT : $V_{DS} \geq V_{GST} \rightarrow V_D - V_S \geq V_{GST}$

$\rightarrow V_D - (-2.5) \geq 1 \rightarrow V_D \geq -1.5$ For SAT.

At maximum signal swing, $V_D = V_D(bias) - \hat{V}_o = 2.5 - \hat{v}_o$

Therefore, $\hat{v}_o \leq 4V$



g_m = 1 mA/V
r_o = 150 kΩ
$1/g_m$ = 1 kΩ

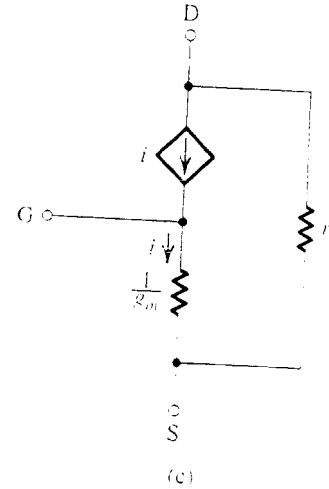


FIGURE E4.30 (Continued)

(3) Common-Source (CS) Amplifier

Fig. 4.3

$$R_{in} = R_G \parallel \infty = R_G$$

$$R_{out} = r_o \parallel R_D$$

$$A_v = \frac{v_o}{v_i} = \frac{-(g_m v_{gs})(r_o \parallel R_D \parallel R_L)}{v_{gs}} = -g_m(r_o \parallel R_D \parallel R_L)$$

$$A_{vo} = -g_m(r_o \parallel R_D)$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}}\frac{v_o}{v_i} = \frac{R_{in}}{R_{in}+R_{sig}} A_v \quad \text{or} \quad -\frac{R_G}{R_G+R_{sig}} g_m(r_o \parallel R_D \parallel R_L)$$

4.32 Consider a CS amplifier based on the circuit analyzed in Exercise 4.30. Specifically, refer to the results of that exercise shown in Fig. E4.30. Find R_{in}, A_{vo}, and R_{out}, both without and with r_o taken into account. Then calculate the overall voltage gain G_v, with r_o taken into account, for the case $R_{sig} = 100$ kΩ and $R_L = 15$ kΩ. If v_{sig} is a 0.4-V peak-to-peak sinusoid, what output signal v_o results?

① R_{in} ② R_{out} ③ A_{vo} with or w/o r_o ; ④ G_v with r_o, $R_{sig}=100K$, $R_L=15K$
⑤ v_o for $V_{sig} = 0.4$ p-p sinusoid

Sol)

With r_o	w/o r_o
① $R_{in} = R_G = 4.7M$	① $R_{in} = R_G = 4.7M$
② $A_{vo} = -g_m(r_o \parallel R_D) = -1\frac{mA}{V}(150K \parallel 15K)$ $= -1mA(13.6K) = -13.64\frac{V}{V}$	② $A_{vo} = -g_m R_D = -15\frac{V}{V}$
③ $R_{out} = r_o \parallel R_D = 150K \parallel 15K = 13.64K\Omega$	③ $R_{out} = R_D = 15K\Omega$

④ $G_v = \frac{R_{in}}{R_{in}+R_{sig}} A_v$, $A_v = -g_m(r_o \parallel R_D \parallel R_L) = -1\frac{mA}{V}(150K \parallel 15K \parallel 15K)$

$= -1\frac{mA}{V}(7.14K) = -7.14\frac{V}{V}$

$G_v = \frac{4.7M}{4.7M+100K}(-7.14\frac{V}{V}) = -7\frac{V}{V}$

⑤ $v_o = 7 \times 0.4V$ p-p $= 2.8V$p-p, DC Bias $V_D = 2.5V$

(4) CS with R_S

Fig. 44

Is S at signal ground or not?

Neglecting r_o

$R_{in} = R_G$

$R_{out} = R_D$

$$A_v = \frac{v_o}{v_i} = \frac{-(g_m v_{gs})(R_D \| R_L)}{v_{gs}\,\frac{\frac{1}{g_m} + R_S}{\frac{1}{g_m}}} = \frac{-g_m(R_D \| R_L)}{1 + g_m R_S}$$

$$A_{vo} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}}\frac{v_o}{v_i} = \frac{R_{in}}{R_{in} + R_{sig}} A_v \quad \text{or} \quad -\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_D \| R_L)}{1 + g_m R_S}$$

4.33 In Exercise 4.32 we applied an input signal of 0.4 V peak-to-peak, which resulted in an output signal of the CS amplifier of 2.8 V peak-to-peak. Assume that for some reason we now have an input signal three times as large as before (i.e., 1.2 V p-p) and that we wish to modify the circuit to keep the output signal level unchanged. What value should we use for R_S?

From x32, CS amp. gave $V_o = 2.8\,V_{p\text{-}p}$ for $V_{sig} = 0.4\,V_{p\text{-}p}$

If $V_{sig} = 1.2\,V_{p\text{-}p}$ and $V_o = 2.8\,V_{p\text{-}p}$, then $R_S = (\quad)$?

Sol)

CS w/o R_S: $V_{sig} = 0.4\,V_{p\text{-}p} \Rightarrow V_o = 2.8\,V_{p\text{-}p} \rightarrow \therefore G_v = \frac{2.8}{0.4} = 7\ \frac{V}{V}$

Note $G_v = -\frac{R_G}{R_G + R_{sig}} g_m(R_L \| R_{out})$

CS With R_S: $V_{sig} = 1.2\,V_{p\text{-}p} \Rightarrow V_o = 2.8\,V_{p\text{-}p} \rightarrow \therefore G_v = \frac{2.8}{1.2} = 2.33\ \frac{V}{V}$

N.B. $G_v = -\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_L \| R_{out})}{1 + g_m R_S}$

$\Rightarrow 1 + g_m R_S = 3 = \frac{7}{2.33}$ Neglecting effect of r_o on R_{out}.

$\therefore R_S = \frac{3-1}{1\,mA/V} = 2\,K\Omega$

(5) Common-Gate (CG) Amplifier

Fig. 45

S is not at signal GND.

Neglecting r_o

$R_{in} = \frac{1}{g_m}$ (low input resistance)

$R_{out} = R_D$ neglecting r_o. (large output resistance)

$$A_v = \frac{V_o}{V_i} = \frac{-(g_m V_{gs})(R_L \| R_{out})}{-V_{gs}} = g_m(R_L \| R_{out}) = g_m(R_L \| R_D) \text{ neglecting } r_o$$

= same as CS amp.

$$G_v = \frac{V_o}{V_{sig}} = \frac{V_i}{V_{sig}} \frac{V_o}{V_i} = \frac{R_{in}}{R_{in}+R_{sig}} A_v = \frac{1/g_m}{1/g_m + R_{sig}} g_m(R_L \| R_{out}) = \frac{g_m(R_L \| R_{out})}{1+g_m R_{sig}}$$

$$= \frac{R_L \| R_{out}}{1/g_m + R_{sig}} \ll \text{CS amp.}$$

Note $i_i = i_o$ $\therefore$ CG = current follower.

4.34 Consider a CG amplifier designed using the circuit of Fig. 4.42, which is analyzed in Exercise 4.30 with the analysis results displayed in Fig. E4.30. Note that $g_m = 1$ mA/V and $R_D = 15$ kΩ. Find R_{in}, R_{out}, A_{vo}, A_v, and G_v for $R_L = 15$ kΩ and $R_{sig} = 50$ Ω. What will the overall voltage gain become for $R_{sig} =$ 1 kΩ? 10 kΩ? 100 kΩ?

① R_{in} ② R_{out} ③ A_v ④ A_{vo} ⑤ G_v for $R_L = 15K\Omega$, $R_{sig} = 50\Omega$, $R_D = 15K$, $g_m = \frac{1mA}{V}$

⑥ G_v for $R_{sig} = 1K$, $10K$, $100K$

Sol) ① $R_{in} = \frac{1}{g_m} = \frac{1}{1mA/V} = 1K\Omega$ ② $R_{out} = R_D = 15K\Omega$

③ $A_v = g_m(R_L \| R_D) = \frac{1mA}{V}(15K \| 15K) = 7.5\frac{V}{V}$ neglecting r_o

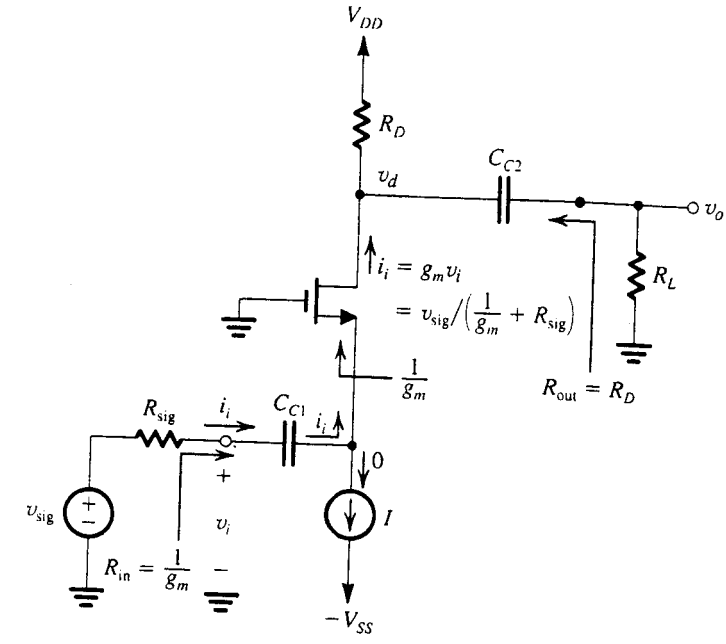
④ $A_{vo} = g_m R_D = \frac{1mA}{V} \cdot 15K = 15\frac{V}{V}$

⑤ $G_v = \frac{R_{in}}{R_{in}+R_{sig}} A_v = \frac{1K}{1K+0.05K} \times 7.5\frac{V}{V} = 0.952 \times 7.5 = 7.14\frac{V}{V}$ for $R_{sig} = 50\Omega$

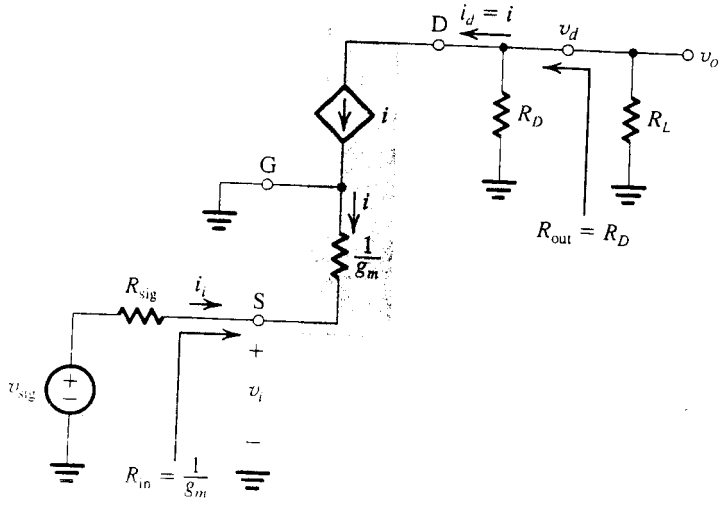
⑥ $G_v = \frac{1K}{1K+1K} 7.5\frac{V}{V} = 0.5 \times 7.5 = 3.75\frac{V}{V}$ for $R_{sig} = 1K$

$G_v = \frac{1K}{1K+10K} 7.5\frac{V}{V} = 0.091 \times 7.5 = 0.68\frac{V}{V}$ for $R_{sig} = 10K$

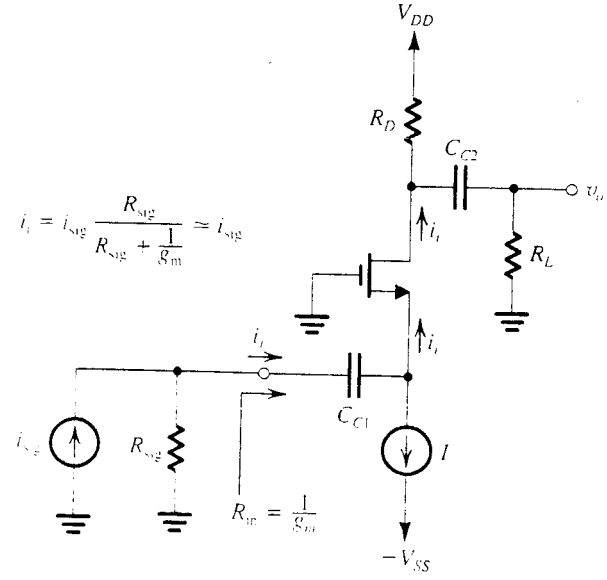
$G_v = \frac{1K}{1K+100K} 7.5\frac{V}{V} = 0.01 \times 7.5 = 0.07\frac{V}{V}$ for $R_{sig} = 100K$



(a)



(b)



(c)

FIGURE 4.45 *(Continued)* (c) The common-gate amplifier fed with a current-signal input.

(6) Common-Drain or Source-Follower

Fig. 46 S is not at signal ground.

$R_{in} = R_G$ because G-to-S is open

R_{out} is not easily determined by Inspection only. For R_{out}, reduce all independent source to zero (incl. V_{sig}) $\rightarrow V_{sig}=0 \rightarrow V_G=0$

$\therefore R_{out} = \frac{1}{g_m} \| r_o \approx \frac{1}{g_m}$

$$A_v = \frac{V_o}{V_i} = \frac{(g_m V_{gs})(r_o \| R_L)}{V_{gs}\frac{1/g_m + r_o \| R_L}{1/g_m}} = \frac{g_m (r_o \| R_L)}{1 + g_m (r_o \| R_L)} = \frac{r_o \| R_L}{1/g_m + r_o \| R_L} \lesssim 1$$

$$A_{vo} = \frac{r_o}{1/g_m + r_o} \rightarrow 1 \quad \therefore \text{S.F.}$$

$$G_v = \frac{V_o}{V_{sig}} = \frac{V_i}{V_{sig}}\frac{V_o}{V_i} = \frac{R_{in}}{R_{in}+R_{sig}} A_v \quad \text{or} \quad \frac{R_G}{R_G + R_{sig}} \frac{r_o \| R_L}{r_o \| R_L + 1/g_m}$$

Source Follower : High R_{in}, Low R_{out}, $A_v \simeq 1$. Use to connect to Source w. high R_{sig} or as output stage of multi-stage amp.

4.35 Consider a source follower such as that in Fig. 4.46(a) designed on the basis of the circuit of Fig. 4.42, the results of whose analysis are displayed in Fig. E4.30. Specifically, note that $g_m = 1$ mA/V and $r_o = 150$ kΩ. Let $R_{sig} = 1$ MΩ and $R_L = 15$ kΩ. (a) Find R_{in}, A_{vo}, A_v, and R_{out} without and with r_o taken into account. (b) Find the overall small-signal voltage gain G_v with r_o taken into account.

$g_m = 1 \frac{mA}{V}$ $r_o = 150K$ $R_G = 4.7M$ $R_{sig} = 1M$ $R_L = 15K$

① R_{in} ② A_v ③ A_{vo} ④ R_{out} w-r-w/o r_o ; ⑤ G_v with r_o

Sol) With r_o

① $R_{in} = R_G = 4.7M$

② $A_v = \frac{r_o \| R_L}{r_o \| R_L + 1/g_m} = \frac{150K \| 15K}{150K \| 15K + 1K} = 0.932 \frac{V}{V}$

③ $A_{vo} = \frac{r_o}{r_o + 1/g_m} = \frac{150K}{150K + 1K} = 0.993 \frac{V}{V}$

④ $R_{out} = r_o \| \frac{1}{g_m} = 152K \| 1K = 0.993K$

W/o r_o

① $R_{in} = R_G = 4.7M$

② $A_v = \frac{R_L}{R_L + 1/g_m} = \frac{15K}{15K + 1K} = 0.938 \frac{V}{V}$

③ $A_{vo} = 1 \frac{V}{V}$

④ $R_{out} = \frac{1}{g_m} = 1K\Omega$

⑤ $G_v = \frac{R_G}{R_G + R_{sig}} A_v = \frac{4.7M}{4.7M + 1M} 0.932 \frac{V}{V} = 0.768 \frac{V}{V}$

(7) Summary of MOS Amps

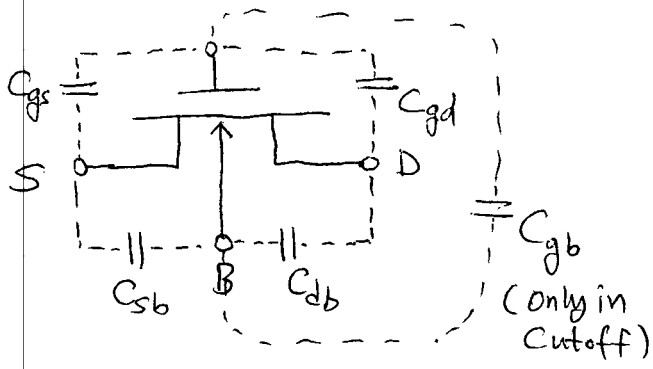
i) CS is used as Gain stage.
One or more CS stages in cascade

ii) CS with R_S : R_S improves many performance factors of CS amp, at the expense of reduced gain

iii) CG :
- Low Rin → only special purpose use as Voltage amp
- Excellent high freq. performance
- Unity gain current follower (low Rin, high Rout) in Cascode

iv) CD or Source Follower
- Voltage buffer (high Rin, low Rout, $A_v \simeq 1$)
- Output stage of multistage amp ($R_{out} = \frac{1}{g_m}$ = low)

4.8 MOS Internal Capacitance

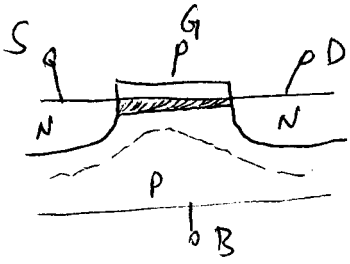


C_{gs}, C_{gd}, C_{gb} = due to C_{ox}

C_{sb}, C_{db} = due to pN junction

1. Gate Capacitance

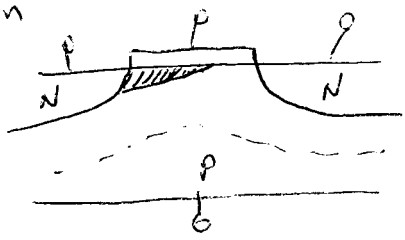
(1) Triode



$C_{gs} = \frac{1}{2} WL C_{ox} = C_{gd}$

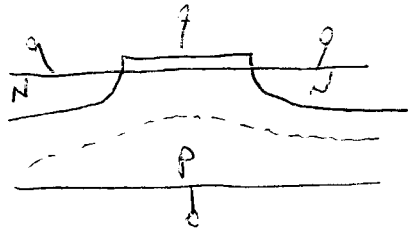
$C_{gb} = 0$

(2) Saturation



$C_{gs} = \frac{2}{3} WL C_{ox}$, $C_{gd} = 0$

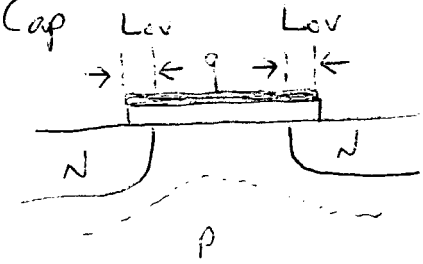
(3) Cutoff



$C_{gs} = 0 = C_{gd}$

$C_{gb} = WL\left(C_{ox}^{-1} + C_{dep}^{-1}\right)^{-1} \approx WL C_{ox}$

(4) Overlap Cap



$C_{ov} = WL_{ov} C_{ox}$

is added to C_{gs}, C_{gd}

2. Junction Capacitence: C_{sb}, C_{db}

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{V_0}}} \qquad C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{V_0}}}$$

4.36 For an *n*-channel MOSFET with t_{ox} = 10 nm, L = 1.0 μm, W = 10 μm, L_{ov} = 0.05 μm, $C_{sb0} = C_{db0}$ = 10 fF, V_0 = 0.6 V, V_{SB} = 1 V, and V_{DS} = 2 V, calculate the following capacitances when the transistor is operating in saturation: C_{ox}, C_{ov}, C_{gs}, C_{gd}, C_{sb}, and C_{db}. (*Note:* You may consult Table 4.1 for values of the physical constants.)

Ans. 3.45 fF/μm^2; 1.72 fF; 24.7 fF; 1.72 fF; 6.1 fF; 4.1 fF

① C_{ox} ② C_{ov} ③ C_{gs} ④ C_{gd} ⑤ C_{sb} ⑥ C_{db} SAT mode

Sol) ① $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-11}\ F/m}{10\times10^{-9}\ m} = 3.45\times10^{-3}\ F/m^2 = 3.45\times10^{-15}\ F/\mu m^2$

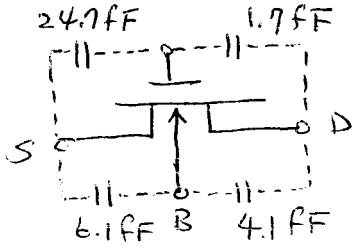
② $C_{ov} = W L_{ov} C_{ox} = 10\times0.05\,\mu m^2 \times 3.45\ fF/\mu m^2 = 1.73\ fF$

③ $C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov} = \frac{2}{3}\times10\,\mu m\times1\,\mu m\times3.45\ fF/\mu m^2 + 1.73\ fF = 24.7\ fF$

④ $C_{gd} = 0 + C_{ov} = 1.73\ fF$ ⑤ $C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{V_0}}} = \frac{10\ fF}{\sqrt{1+\frac{1}{0.6}}} = 6.12\ fF$

⑥ C_{dB}: $V_{DB} = V_{DS} + V_{SB} = 2+1 = 3V$

$$C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{V_0}}} = \frac{10}{\sqrt{1+\frac{3}{0.6}}} = 4.08\ fF$$

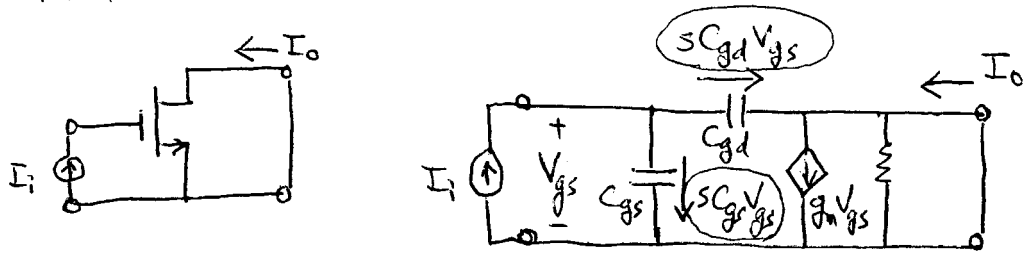


3. High Freq. Model of MOSFET

Fig. 4.7

4. MOSFET f_T

Find short-circuit current gain for sinusoid input



$$I_i = s(C_{gs}+C_{gd})V_{gs} \qquad I_o = (g_m - sC_{gd})V_{gs} \approx g_m V_{gs}$$

$$\therefore \frac{I_o}{I_i} = \frac{g_m}{s(C_{gs}+C_{gd})} \equiv \frac{\omega_T}{s}$$

Note $\left|\frac{I_o}{I_i}\right| = 1$ at $\omega = \omega_T$

$$\boxed{\omega_T \equiv \frac{g_m}{C_{gs}+C_{gd}} = 2\pi f_T}$$

4.37 Calculate f_T for the n-channel MOSFET whose capacitances were found in Exercise 4.36. Assume operation at 100 μA, and that $k_n' = 160\ \mu A/V^2$.

Ans. 3.7 GHz

$f_T = (\quad)$ for $I_d = 100\,mA$, $K_n' = 160\ \frac{\mu A}{V^2}$

From x36, $C_{gs} = 24.7\,fF$, $C_{gd} = 1.7\,fF$, $W = 10\,mm$, $L = 1\,mm$

Sol) $g_m = \sqrt{2K_n'\frac{W}{L}I_d} = \sqrt{2\times 0.16\times\frac{10}{1}\times 0.1} = 0.566\ \frac{mA}{V}$

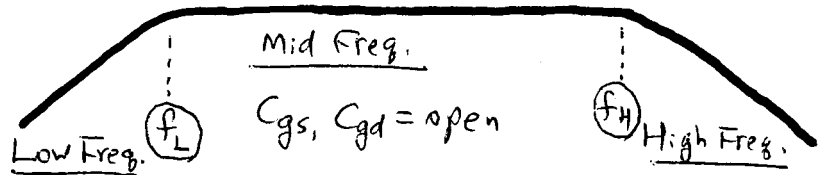
$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}} = \frac{1}{2\pi}\frac{0.566\ \frac{mA}{V}}{(24.7+1.7)fF} = 3.41\times 10^9\ Hz$$

Note basic result is for $\frac{W}{L} = 12$

4.9 Frequency Response of CS Amp.

$A_M = G_v$ @ mid freq.

Fig. 49



Mid Freq.
C_{gs}, C_{gd} = open
C_{c_1}, C_{c_2}, C_s = short

Low Freq.
C_{gs}, C_{gd} = open
C_{c_1}, C_{c_2}, C_s = give f_L

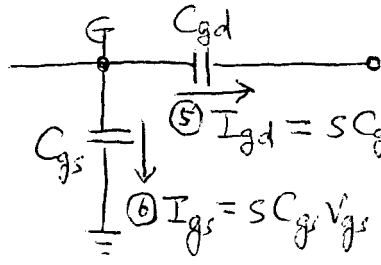
High Freq.
C_{gs}, C_{gd} = give f_H
C_{c_1}, C_{c_2}, C_s = short

$$BW = f_H - f_L \simeq f_H$$

(1) f_H

Fig. 50

Transistor internal capacitors, C_{gs} and C_{gd}, make a Low-Pass filter $\longrightarrow$ f_H



⑤ $I_{gd} = sC_{gd}(V_{gs} - V_o) = sC_{gd}(V_{gs} + g_m V_{gs} R_L') = sC_{gd}(1 + g_m R_L')V_{gs}$

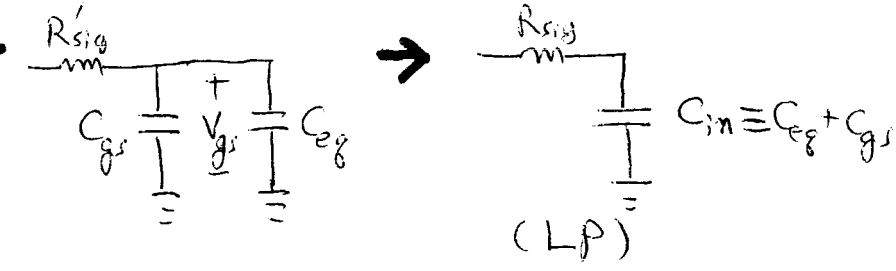
⑥ $I_{gs} = sC_{gs}V_{gs}$

$I_{gd} \equiv sC_{eq}V_{gs}$

"Miller Effect"

$C_{eq} \equiv C_{gd}(1 + g_m R_L')$

$= C_{gd}(1 + |A_v|)$



→ R'_{sig} and C_{in} form a Low-Pass network

$$f_H = \frac{1}{2\pi} \frac{1}{R'_{sig} C_{in}}$$

where, $R'_{sig} = R_{sig} \| R_G$ = "R seen by C_{in} looking back toward signal source"

$C_{in} = C_{gs} + C_{eq} = C_{gs} + C_{gd}(1 + g_m R_L')$

↑ Cap connecting (in) to (out)

(2) f_L Fig 5.1

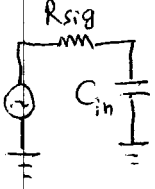
External Capacitors make High-Pass networks.

- $R_{sig} - C_{C_1} - R_G$: $2\pi f_{p_1} = \dfrac{1}{C_{C_1}(R_{sig}+R_G)}$
- $\dfrac{1}{g_m} - C_S$: $2\pi f_{p_2} = \dfrac{1}{C_S \cdot \frac{1}{g_m}}$
- $R_D - C_{C_2} - R_L$: $2\pi f_{p_3} = \dfrac{1}{C_{C_2}(R_D+R_L)}$

4.38 For the CS amplifier specified in Example 4.12, find the values of A_M and f_H that result when the signal-source resistance is reduced to 10 kΩ.

$R_G = 4.7M$ $R_D = R_L = 15K$ $g_m = 1\frac{mA}{V}$ $r_o = 150K$ $C_{gs} = 1pF$ $C_{gd} = 0.4pF$
$R_{sig} = 10K$ ① A_m ② f_H

Sol) ① $A_M = -\dfrac{R_G}{R_G+R_{sig}} g_m (r_o \| R_D \| R_L) = -\dfrac{4.7M}{4.7M+0.01M} \cdot 1\,(150\|15\|15) = -7.12\frac{V}{V}$



$C_{eq} = C_{gd}(1+g_m R_L') = 0.4p(1+1\times 7.14) = 3.256\,pF$

$C_{in} = C_{gs} + C_{eq} = 1pF + 3.25pF = 4.256pF$, $R_{sig}' = R_{sig} \| R_G \simeq 0.01M$

② $f_H = \dfrac{1}{2\pi}\dfrac{1}{C_{in} \times R_{sig}'} = \dfrac{1}{2\pi}\dfrac{1}{4.26f \times 0.01M} = 3.74\,mHz$

4.40 A CS amplifier has $C_{C1} = C_S = C_{C2} = 1\,\mu F$, $R_G = 10\,M\Omega$, $R_{sig} = 100\,k\Omega$, $g_m = 2\,mA/V$, $R_D = R_L = 10\,k\Omega$. Find A_M, f_{P1}, f_{P2}, f_{P3}, and f_L.

① A_m ② f_{p_1} ③ f_{p_2} ④ f_{p_3} ⑤ f_L

Sol) ① $A_m = -\dfrac{R_G}{R_G+R_{sig}} g_m (r_o \| R_D \| R_L) = -\dfrac{10M}{10M+0.1M} 2m\,(10K\|10K) = -10\frac{V}{V}$

② $f_{p_1} = \dfrac{1}{2\pi}\dfrac{1}{C_{C_1}(R_{sig}+R_G)} = \dfrac{1}{2\pi}\dfrac{1}{1\mu(0.1M+10M)} = 0.016\,Hz$

③ $f_{p_2} = \dfrac{1}{2\pi}\dfrac{1}{C_S \frac{1}{g_m}} = \dfrac{1}{2\pi}\dfrac{1}{1\mu \times 0.5K} = 318.3\,Hz$

④ $f_{p_3} = \dfrac{1}{2\pi}\dfrac{1}{C_{C_2}(R_D+R_L)} = \dfrac{1}{2\pi}\dfrac{1}{1\mu(10K+10K)} = 7.96\,Hz$

⑤ $f_L \cong \max(f_{p_1}, f_{p_2}, f_{p_3}) = f_{p_2} = 318.3\,Hz$

4.12 SPICE MOSFET Parameters

LEVEL = particular model ex) LEVEL=1 simplest model

$$I_d = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_t)^2$$

TABLE 4.7 Parameters of the SPICE Level-1 MOSFET Model (Partial Listing)

SPICE Parameter	Book Symbol	Description	Units
		Basic Model Parameters	
LEVEL		MOSFET model selector	
TOX	t_{ox}	Gate-oxide thickness	m
COX	C_{ox}	Gate-oxide capacitance, per unit area	F/m^2
UO	μ	Carrier mobility	$cm^2/V \cdot s$
KP	k'	Process transconductance parameter	A/V^2
LAMBDA	λ	Channel-length modulation coefficient	V^{-1}
		Threshold Voltage Parameters	
VTO	V_{t0}	Zero-bias threshold voltage	V
GAMMA	γ	Body-effect parameter	$V^{1/2}$
NSUB	N_A, N_D	Substrate doping	cm^{-3}
PHI	$2\Phi_f$	Surface inversion potential	V
		MOSFET Diode Parameters	
JS		Body-junction saturation-current density	A/m^2
CJ		Zero-bias body-junction capacitance, per unit area over the drain/source region	F/m^2
MJ		Grading coefficient, for area component	
CJSW		Zero-bias body-junction capacitance, per unit length along the sidewall (periphery) of the drain/source region	F/m
MJSW		Grading coefficient, for sidewall component	
PB	V_0	Body-junction built-in potential	V
		MOSFET Dimension Parameters	
LD	L_{ov}	Lateral diffusion into the channel from the source/drain diffusion regions	m
WD		Sideways diffusion into the channel from the body along the width	m
		MOS Gate-Capacitance Parameters	
CGBO		Gate-body overlap capacitance, per unit channel length	F/m
CGDO	C_{ov}/W	Gate-drain overlap capacitance, per unit channel width	F/m
CGSO	C_{ov}/W	Gate-source overlap capacitance, per unit channel width	F/m

Junction Capacitance : S--B, D-B

$$C_{db} = \frac{\text{CJ}}{\left(1 + \frac{V_{DB}}{\text{PB}}\right)^{\text{MJ}}} \text{AD} + \frac{\text{CJSW}}{\left(1 + \frac{V_{DB}}{\text{PB}}\right)^{\text{MJSW}}} \text{PD}$$

$$C_{sb} = \frac{\text{CJ}}{\left(1 + \frac{V_{SB}}{\text{PB}}\right)^{\text{MJ}}} \text{AS} + \frac{\text{CJSW}}{\left(1 + \frac{V_{SB}}{\text{PB}}\right)^{\text{MJSW}}} \text{PS}$$

Overlap Cap

$$C_{gs,ov} = W\,\text{CGSO}$$

$$C_{gd,ov} = W\,\text{CGDO}$$

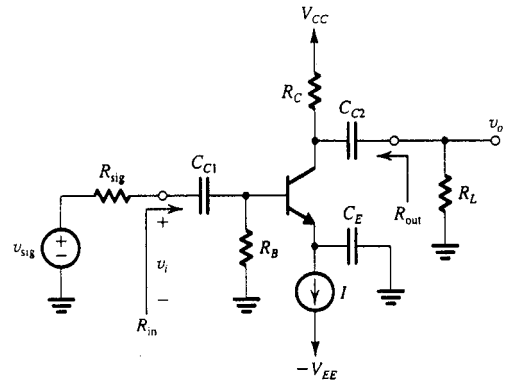
$$C_{gb,ov} = L\,\text{CGBO}$$

Effective L, W

$$L_{\text{eff}} = L - 2\text{LD}$$

$$W_{\text{eff}} = W - 2\text{WD}$$

Common Emitter



$$R_{in} = R_B \| r_\pi = R_B \| (\beta+1) r_e$$

$$A_v = -g_m(r_o \| R_C \| R_L)$$

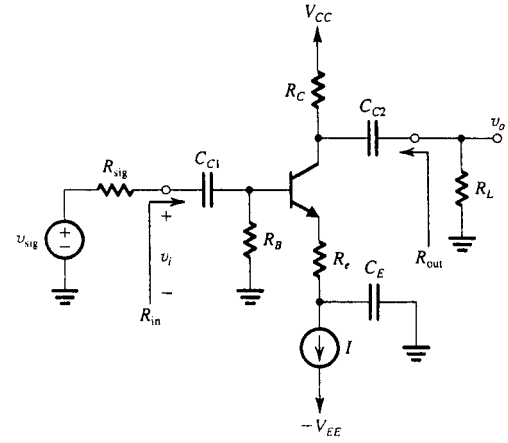
$$R_{out} = r_o \| R_C$$

$$G_v = -\frac{(R_B \| r_\pi)}{(R_B \| r_\pi) + R_{sig}} g_m (r_o \| R_C \| R_L)$$

$$\cong -\frac{\beta(r_o \| R_C \| R_L)}{r_\pi + R_{sig}}$$

$$A_{is} = -g_m R_{in} \cong -\beta$$

Common Emitter with Emitter Resistance



Neglecting r_o:

$$R_{in} = R_B \| (\beta+1)(r_e + R_e)$$

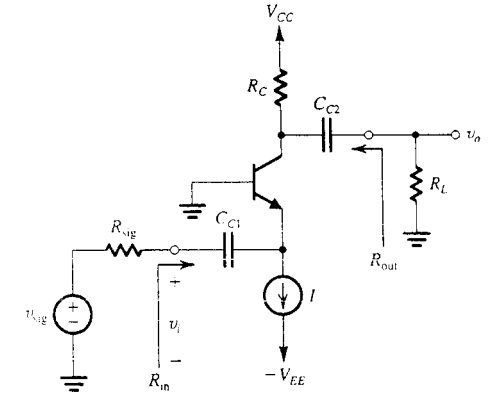
$$A_v = -\frac{\alpha(R_C \| R_L)}{r_e + R_e} \cong \frac{-g_m(R_C \| R_L)}{1 + g_m R_e}$$

$$R_{out} = R_C$$

$$G_v \cong -\frac{\beta(R_C \| R_L)}{R_{sig} + (\beta+1)(r_e + R_e)}$$

$$\frac{v_\pi}{v_i} \cong \frac{1}{1 + g_m R_e}$$

Common Base



Neglecting r_o:

$$R_{in} = r_e$$

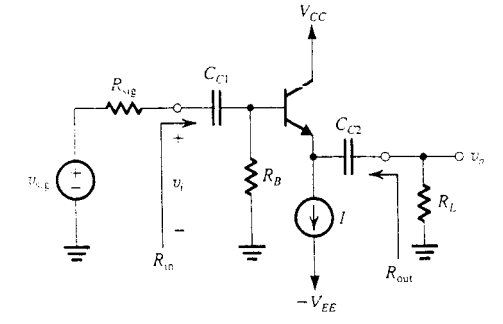
$$A_v = g_m(R_C \| R_L)$$

$$R_{out} = R_C$$

$$G_v = \frac{\alpha(R_C \| R_L)}{R_{sig} + r_e}$$

$$A_{is} \cong \alpha$$

Common Collector or Emitter Follower



$$R_{in} = R_B \| (\beta+1)[r_e + (r_o \| R_L)]$$

$$A_v = \frac{(r_o \| R_L)}{(r_o \| R_L) + r_e}$$

$$R_{out} = r_o \| \left[r_e + \frac{R_{sig} \| R_B}{\beta+1} \right]$$

$$G_v = \frac{R_B}{R_B + R_{sig}} \frac{(r_o \| R_L)}{\frac{R_{sig} \| R_B}{\beta+1} + r_e + (r_o \| R_L)}$$

$$A_{is} \cong \beta+1$$