Enhancement-Mode N-Polar GaN MISFETs With Self-Aligned Source/Drain Regrowth

Uttam Singisetti, Man Hoi Wong, Sansaptak Dasgupta, Nidhi, Brian Swenson, Brian J. Thibeault, James S. Speck, and Umesh K. Mishra

***Abstract*—We report gate-first enhancement-mode (E-mode) N-polar GaN MISFET devices with self-aligned source/drain regions by molecular beam epitaxy regrowth and with a SiN_x gate dielectric. E-mode operation at $V_{ds} = 4.0$ V is demonstrated for devices with gate lengths > 0.18 μm with a 20-nm GaN channel and a high-temperature SiN_x gate dielectric. A high drain current of 0.74 A/mm was measured for an $L_g = 0.62$-μm device with a peak transconductance of 225 mS/mm and a positive threshold voltage of 1 V. The on resistance of the device was 2 $\Omega \cdot$ mm. Devices show short-channel effect with decreasing gate lengths.**

***Index Terms*—Enhancement-mode GaN HEMT, MISFET, MIS-HEMT, N-polar GaN, self-aligned FET.**

I. Introduction

POLARIZATION-INDUCED GaN channel 2-D electron gas (2DEG) high-electron-mobility transistors with high $f_t(\sim 206$ GHz), $f_{\max}(\sim 300$ GHz) and high breakdown voltage have been demonstrated with applications in micro- and millimeter-wave power amplifiers [1]–[4]. These devices are typically depletion mode (D-mode). There is a growing interest in high-performance enhancement-mode (E-mode) GaN channel devices because of single voltage operation and simpler circuit topologies. Typical methods to obtain E-mode GaN FETs are gate recess etch, thin gate barrier layers, and F^- ion treatment [5]–[9]. Ga-polar (0001) E-mode GaN channel devices with good dc and high-frequency performance have been demonstrated [6], [8]. However, the use of alloyed contacts through wide-bandgap barrier layers may lead to higher source/drain contact resistances, subsequently high source access resistances (R_s), and high on resistances $(R_{\rm on})$. Recently, N-polar GaN MISFET devices were demonstrated with a record-high $f_t \cdot L_g$ product of 16.8 GHz $\cdot$ μm at a gate length of 130 nm through aggressive reduction of parasitic source access and contact resistances [10]. The advantages of E-mode GaN FETs fabricated on N-polar GaN include the regrowth of the n^+ source/drain regions for reduced access resistance and the wide-bandgap bottom barrier layers used for polarization doping of the channel. They can also be integrated with high-performance N-polar D-mode devices to enable novel circuit functionalities.

Here, we report E-mode N-polar GaN FETs fabricated with a gate-first process with self-aligned regrown source/drain regions and nonalloyed ohmic contacts for low access resistances. These devices show a peak drive current (I_d) of 0.74 A/mm and a peak transconductance (g_m) of 225 mS/mm at $L_g = 0.62$ μm with a threshold voltage $(V_{\rm th})$ of 1.0 V and a low on resistance of 2 $\Omega \cdot$ mm. The gate length dependence of the device parameters is also explored, and the devices show threshold-voltage roll-off caused by drain-induced barrier lowering (DIBL).

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II. Device Structure and Fabrication

Fig. 1 shows the cross-sectional schematic and band diagrams of the self-aligned device with source/drain regrowth. The source access distance $(L_{\rm SG})$ in the self-aligned devices is given by the well-controlled plasma-enhanced chemical vapor deposition (PECVD) SiN_x sidewall thickness, greatly reducing the source access resistance. The GaN channel is 20 nm thick with a 2-nm AlN back barrier. The E-mode operation of the device is enabled by the polarization-induced field of a 2-nm AlN capping layer which depletes the 2DEG [Fig. 1(c)]. Removal of the AlN layer from the access regions recovers the 2DEG induced by the bottom AlN layer [Fig. 1(d)], which is necessary for low regrowth interfacial resistance. We developed a selective UV–ozone–BHF digital wet etch process, by which 2 nm of N-polar AlN is completely removed in four cycles of 5-min UV–ozone and 30-s BHF with no appreciable etching of the GaN channel as verified with XPS. The bottom-AlN polarization-induced 2DEG in the access region, the n^+ regrowth, and the SiN_x sidewall thickness are the three variables for controlling the source access resistance, increasing the design space for the E-mode N-polar GaN devices.

The devices were grown by plasma-assisted molecular beam epitaxy (MBE) on C-face SiC substrates to obtain N-polarity. An AlN nucleation layer, followed by a two-step GaN buffer, was adopted for growing a high-quality semi-insulating buffer. Device fabrication began with deposition of 5 nm of high-temperature CVD SiN_x as a gate dielectric, which has been used as a gate dielectric layer in previously reported N-polar devices [10], [11]. Sputtered W(50-nm)/Cr(50-nm)/ Ar-sputtered-SiN_x(300-nm) gates with $L_g = 0.18-10$ μm were defined by electron beam lithography. An alternating selective dry etch scheme minimized etch damage to the channel following the process in [12] and [13]. The gate stack was modified from the previously reported W/Cr/SiO_2[12], [13] gate stack, with

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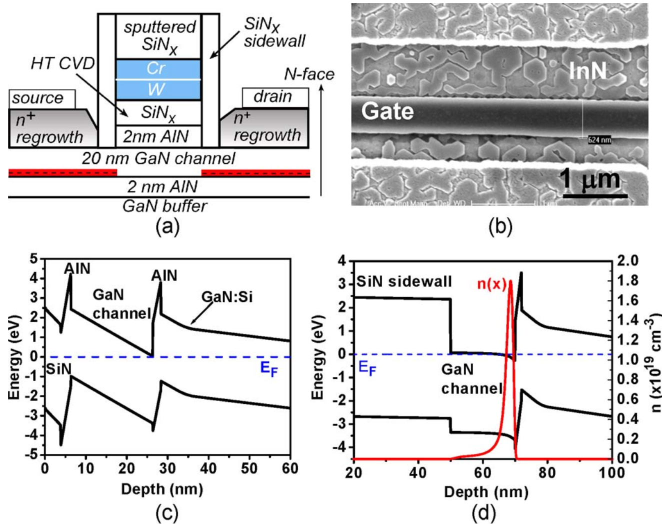

Fig. 1. (a) Device cross-sectional schematic. (b) Top view SEM of the device after source/drain regrowth. (c) Band diagram under the gate showing E-mode operation. (d) Band diagram under the SiN_x sidewall access region.

SiO_2 being replaced by the Ar-sputtered-SiN_x layer to have selectivity with the AlN wet etch. The AlN layer in the access region was then selectively etched, and 50 nm of PECVD SiN_x sidewalls was formed. Hall measurement on process monitor samples shows a 2DEG density 3×10^{12} cm^{-2} with a mobility of 650 cm^2/V $\cdot$ s after AlN removal. The 2DEG density and mobility after 50 nm of PECVD SiN_x deposition [Fig. 1(d)] are 4.5×10^{12} cm^{-2} and 1060 cm^2/V $\cdot$ s, respectively, with a sheet resistance (R_{sh}) of 1300 $\Omega/\square$. The 2DEG in the access region under the SiN_x sidewall has a similar role as the source/drain overlap implanted region in a Si MOSFET. Next, a graded n$^+$ InGaN (40 nm) doped with $[\mathrm{Si}] = 2 \times 10^{19}$ cm^{-3} and a top InN (10 nm) contact layer are regrown by plasma-assisted MBE to reduce the access and contact resistances [14]. Nonalloyed Ti/Au/Ni contacts are formed for the source/drain regions which have been shown to give a low contact resistance of 0.027 $\Omega \cdot$ mm to the 2DEG [14].

III. Results and Discussion

The input and output dc characteristics of a 0.62-μm-gate-length FET (Fig. 2) show E-mode operation with a V_{th} of 1.0 V and a maximum I_{ds} of 0.74 A/mm at $V_{\mathrm{gs}} = 5.0$ V and $V_{\mathrm{ds}} = 4.0$ V. Unlike what has been observed in Ga-polar AlN/GaN heterostructures [15], the deposition of SiN_x dielectric does not lead to D-mode behavior. The peak g_m values are 225 and 120 mS/mm at $V_{\mathrm{ds}} = 4.0$ and 0.5 V, respectively. A high gate leakage current of 7.4 mA/mm is measured at $V_{\mathrm{gs}} = 5.0$ V and $V_{\mathrm{ds}} = 4.0$ V because of the forward leakage through the 5-nm-thick SiN_x gate dielectric. No current collapse is observed in 200-ns-pulsed I–V measurement. Small-signal measurement of the device shows an extrinsic f_t of 18 GHz. Fig. 3(a) shows the input characteristics of a 0.18-μm-gate-length device showing a D-mode behavior. The threshold voltage measured by the linear extrapolation of the I_{ds}–V_{gs} plot at $V_{\mathrm{ds}} = 4.0$ V rolls off with decreasing gate lengths, and the device becomes D-mode at $L_g = 0.18$ μm and $V_{\mathrm{ds}} = 4.0$ V due to short-channel effects caused by the low aspect ratio at $L_g = 0.18$ μm and self-aligned drain. Similar DIBL-induced threshold-voltage reduction has been observed in previously reported E-mode devices in [6].

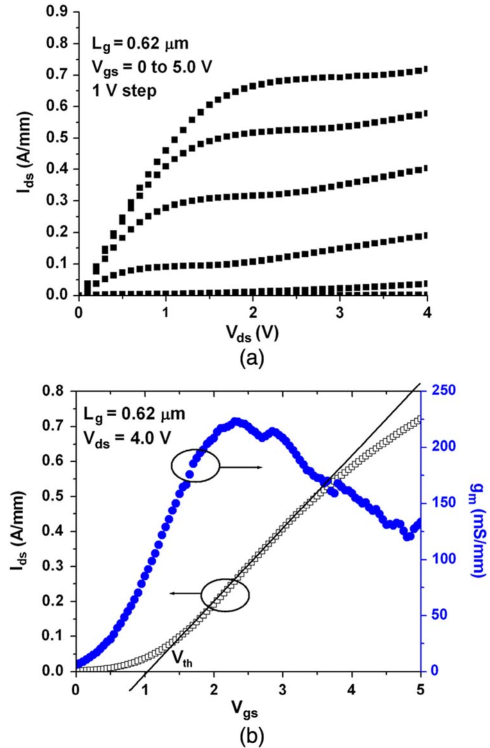

Fig. 2. Common-source output and input characteristics of a self-aligned 0.62-μm-gate-length device.

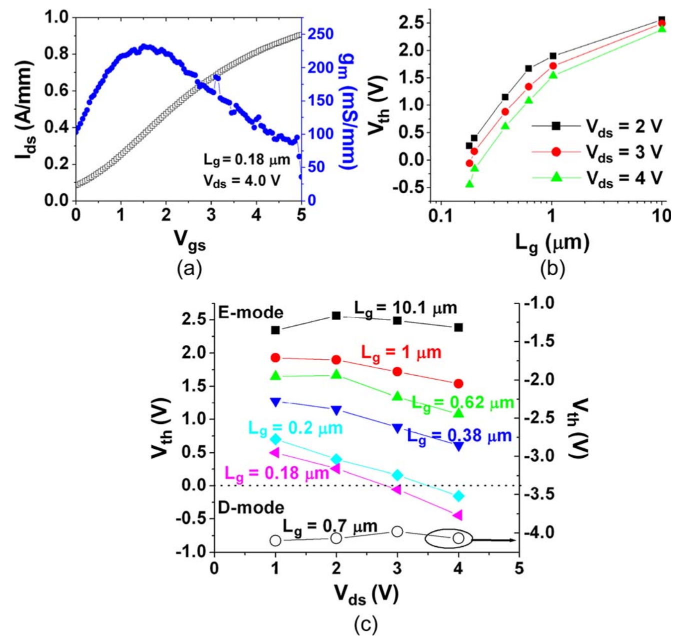

Fig. 3. (a) Input characteristics at $V_{\mathrm{ds}} = 4.0$ V for a 0.18-μm-length device. (b) Threshold-voltage roll-off with decreasing gate length and (c) increasing drain bias. The open circles (right Y-axis) in (c) show the V_{th} for a non-self-aligned D-mode device. The gate lengths of the devices were measured by SEM.

The threshold voltages of the devices for different gate lengths and drain biases are shown in Fig. 3(b) and (c). The threshold-voltage roll-off caused by DIBL is more severe in shorter gate lengths and at higher drain biases. The V_{th} for an $L_g = 0.7$-μm non-self-aligned D-mode device without source/drain regrowth and of comparable aspect ratio is also shown in Fig. 3(c), which shows less DIBL effect. The observed V_{th} roll-off is

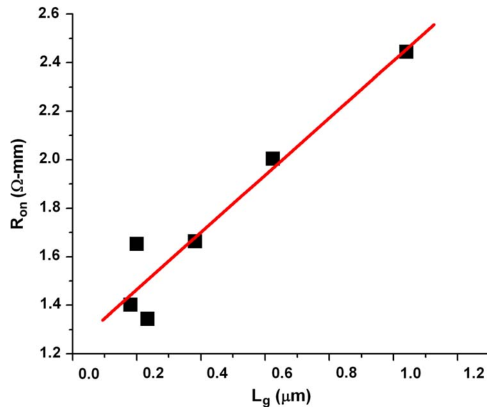

Fig. 4. Device on resistance versus gate length. A total source/drain parasitic access resistance of 1.2 $\Omega \cdot$ mm is extracted from the linear interpolation to zero gate length.

faster than the reported V_{th} roll-off in Ga-polar devices with comparable barrier thicknesses [16]. The self-aligned n^+ drain is the probable cause for the faster V_{th} roll-off in the devices presented here. Thus, in order to obtain high RF performance in sub-100-nm-gate-length E-mode devices, the vertical dimension of the device needs to be scaled along with the gate length to keep the device aspect ratio high.

A low on resistance (R_{on}) of 2.0 $\Omega \cdot$ mm at $L_g = 0.62$ μm is obtained because of the self-aligned structure. From the linear extrapolation of the zero-bias on resistance versus gate length to zero gate lengths (Fig. 4), a 0.6-$\Omega \cdot$ mm source access resistance is determined, which gives an intrinsic g_m of 260 mS/mm. The transfer length method (TLM) patterns on the n^+ graded InGaN/InN regrown on the GaN channel material showed 540-$\Omega/\square$ sheet resistance and 0.04-$\Omega \cdot$ mm lateral contact resistance without removing the regrown material between the TLM pads. With a source-contact-to-gate separation of 0.77 μm [verified by scanning electron microscopy (SEM)], the contribution of this region to the source resistance is 0.41 $\Omega \cdot$ mm. The contribution of the 50-nm SiN_x sidewall region calculated from the measured Hall sheet resistance is 0.065 $\Omega \cdot$ mm. Adding the contact resistance of 0.04 $\Omega \cdot$ mm from the TLM measurement, a source resistance of 0.51 $\Omega \cdot$ mm is calculated. The difference of 0.09 $\Omega \cdot$ mm between the source resistance calculated earlier and the source access resistance extrapolated from the device on resistance versus gate length plot could be the regrowth interfacial resistance.

Although the devices show low parasitic resistances, they also show limitations in the OFF state. The I_{on} $(V_{\mathrm{gs}} = 5.0\ \mathrm{V}, V_{\mathrm{ds}} = 4.0\ \mathrm{V})/I_{\mathrm{off}}$ $(V_{\mathrm{gs}} = 0.0\ \mathrm{V}, V_{\mathrm{ds}} = 4.0\ \mathrm{V})$ ratio of the $L_g =$ 0.62-μm device is 720, and the I_{on} $(V_{\mathrm{gs}} = 5.0\ \mathrm{V}, V_{\mathrm{ds}} = 4.0\ \mathrm{V})/I_{\mathrm{off}}$ $(V_{\mathrm{gs}} = 0.0\ \mathrm{V}, V_{\mathrm{ds}} = 0.5\ \mathrm{V})$ is 4×10^4. The three-terminal breakdown voltage of the device at $V_{\mathrm{gs}} = 0.0\ \mathrm{V}$ $(V_{\mathrm{ds,br}})$ is 15 V. Drain field engineering and asymmetric low-doped drain regrowth technology could lead to increased V_{ds} operation and increased drain breakdown voltages.

In conclusion, we have demonstrated for the first time a self-aligned GaN E-mode MISFET technology with good dc performance and low parasitic resistances. The devices show poor pinchoff and high gate leakage. Vertical scaling of the channel and incorporating a gate dielectric with low leakage are required to improve the OFF-state performance and gate leakage of the devices. This baseline device layer structure offers flexibility in threshold-voltage engineering in scaled devices through controlling the electrostatics contributed by the back barrier, the GaN channel, and the AlN capping layer. The gate length scalability of the present epitaxial structure is limited because of the low aspect ratio. Further vertical scaling is necessary to scale the gate length to sub-100-nm dimensions.

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