Scalable E-mode N-polar GaN MISFET devices and process with self-aligned source/drain regrowth

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E-mode GaN FETs fabricated on N-polar GaN have several unique scaling advantages such as vertical scaling of channel with back barrier for better electron confinement and regrowth of the n^+ source/drain regions for reduced access resistance. They can also be integrated with recently demonstrated high performance N-polar D-mode [1] devices enabling novel circuit functionalities. Ga-polar E-mode devices with good performance have been demonstrated [2]; however in these devices source/drain contacts are invariably made to wideband gap $Al_xGa_{1-x}N$ barriers leading to higher contact resistances which considerably limit the aggressive scaling of the device. Here we report E-mode N-polar GaN FETs fabricated with a scalable gate first process with self-aligned regrown source/drain regions and non-alloyed ohmic contacts for low access resistances. These devices show a peak drive current (I_d) of 0.74 A/mm and peak transconductance (g_m) of 250 mS/mm at L_g = 0.55 μm with a threshold voltage (V_{th}) of 0.8 V.

Figs. 1-3 show the cross-section schematic and band diagrams of the self-aligned device. The devices were grown by plasma-assisted MBE on C-face SiC substrates to obtain N-polarity. An AlN nucleation layer followed by a two-step GaN buffer scheme were adopted for growing a high quality, semi-insulating buffer. The channel is 20 nm thick with 2 nm AlN back barrier. E-mode operation of the device is enabled by the polarization induced field of a 2 nm AlN capping layer which depletes the two-dimensional electron gas (2DEG) (Fig. 2). The AlN layer needs to be removed from the access regions for recovering the 2-DEG (Fig. 3) and for low regrowth interfacial resistance. Therefore, a high selective etch of AlN over GaN with low damage to the channel is critical. A wet etch process is preferred for low damage but the high reactivity of N-polar III-Ns makes it challenging to find suitable selective etchants. We developed a selective UV-Ozone-BHF digital wet etch process, by which 2 nm of N-polar AlN is completely removed in four cycles of 5-minute UV-Ozone and 30-second BHF with no appreciable etching of the GaN channel as verified with XPS (Fig. 4). This etch enables scaling of the GaN channel to sub-5 nm thicknesses necessary for highly scaled gate lengths.

Device fabrication began with deposition of 5 nm of high temperature CVD SiN_x as a gate dielectric. Sputtered W(50nm)/Cr(50nm)/SiN_x(300nm) gates with L_g = 0.23μm–10μm were defined in an alternating dry etch scheme minimizing etch damage to the channel following the process in reference [3]. The gate stack was modified from the previously reported W/Cr/SiO_2 gate stack by incorporating sputter SiN_x layer to have selectivity with the AlN wet etch. The AlN layer in the access region was then selectively etched and 50 nm of PECVD SiN_x sidewalls were formed. The layer structure is designed so that that the access region under the sidewall has 4.5×10^{12} cm^{-2} charge as verified by Hall test structures (Fig. 3), giving a R_{sh} of 1300 Ω/□. A graded n^+ InGaN (40 nm) /InN (10nm) contact layer is regrown by plasma-MBE to reduce the access and contact resistances (Fig. 5) [4].

The DC characteristics of a 0.55μm gate length FET (Figs. 6-8) show E-mode operation with a V_{th} of 0.8 V and a maximum I_{ds} of 0.74 A/mm at V_{gs}=5.0 V and V_{ds}=4.0V. Unlike what has been observed in Ga-polar AlN/GaN heterostructures, the deposition of SiN_x dielectric does not lead to D-mode behavior [5]. The peak g_m values are 250 mS/mm and 120 mS/mm at V_{ds} = 4.0 V and V_{ds} = 0.5 V respectively. A gate leakage current of 7.4 mA/mm is measured at V_{gs} = 5.0 V and V_{ds} = 4.0 V. Small-signal measurement of the device showed an extrinsic f_t of 18 GHz (Fig. 12). Fig. 9 shows the input characteristics of devices with gate lengths 10 μm to 0.23 μm. The threshold voltage measured by the linear extrapolation of I_{ds}-V_{gs} plot at V_{ds} = 4.0V, rolls off with decreasing gate lengths (Fig. 10) and the device becomes D-mode at L_g = 0.23 μm, due to short channel effects caused by the low aspect ratio at L_g = 0.23 μm and self-aligned drain. From measurements of zero-bias on-resistance (Fig. 11), a 1.0 Ω–mm source access resistance is determined, which gives an intrinsic g_m of 330 mS/mm. The TLM patterns on the n^+ graded InGaN/InN regrown on the GaN channel material showed 1000 Ω/□ sheet resistance and 0.2 Ω–mm lateral contact resistance without removing the regrown material between the TLM pads. The higher-than-expected contact and access sheet resistance compared to those reported in D-mode devices with source/drain regrowth [1] could be due to low surface coverage of InN as seen in SEM. Further optimization of the regrowth conditions will solve the problem.

In conclusion, we have demonstrated for the first time a self-aligned and scalable GaN E-mode MISFET technology with good performance. This baseline device layer structure offers flexibility in threshold voltage engineering in scaled devices through controlling the electrostatics contributed by the back barrier, GaN channel and the AlN capping layer. The gate length scalability of the present epitaxial structure is limited because of the low aspect ratio. Vertical scaling of the channel and incorporation of high-k dielectrics are the pathways to scale the device to sub-100 nm gate lengths for high frequency applications.

This work was supported by DARPA NeXT program, ONR-MINE MURI (Dr P. Maki, Dr H. Dietrich) and Intel Corporation. A portion of this work was performed in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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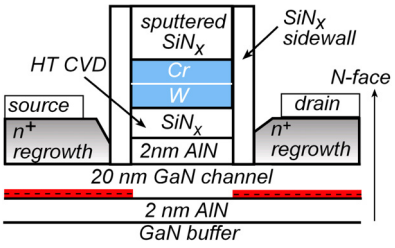

Fig. 1: Cross-section schematic of the self-aligned N-polar GaN MISFET (not to scale).

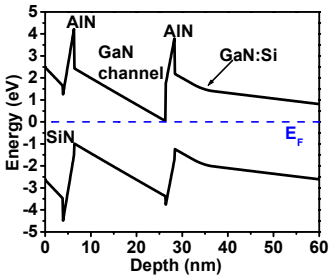

Fig. 2. Band diagram under the gate showing E-mode operation.

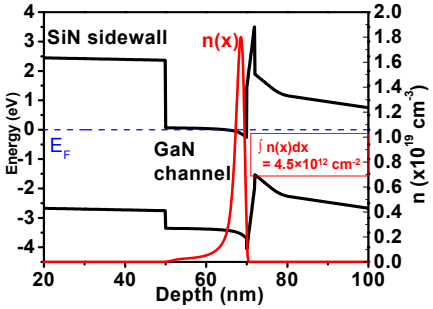

Fig. 3: Band diagram under the sidewall access regions, 4.5×10^{12} cm^{-2} 2-DEG density was verified by Hall.

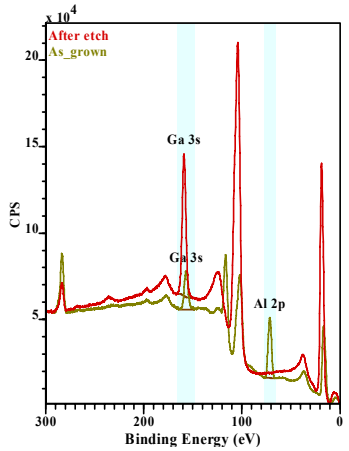

Fig. 4: XPS of the device before and after AlN etch. The Al2p signal is absent after four cycles of etching.

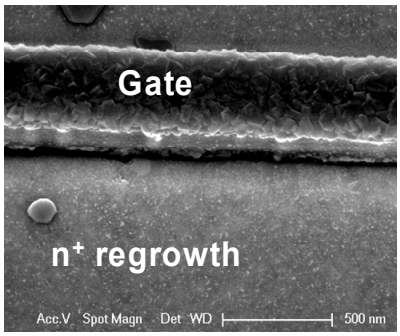

Fig. 5: Top view SEM of the gate showing self-aligned n^+ regrowth.

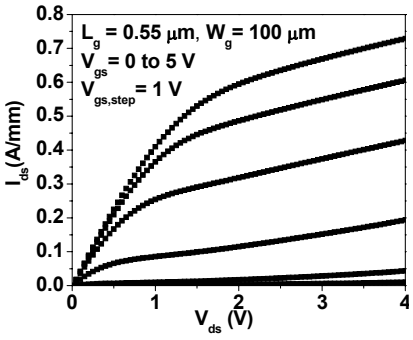

Fig. 6: I_{ds}-V_{ds} plot of 0.55 µm gate length device.

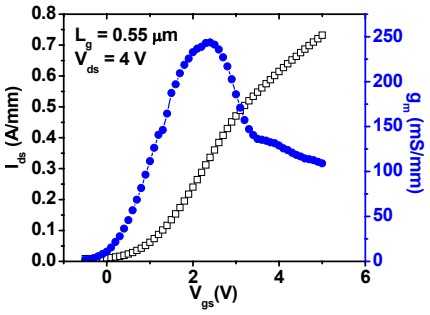

Fig. 7: I_{ds}-V_{gs} and g_m-V_{gs} plot of 0.55 µm gate length device at V_{ds} = 4.0 V.

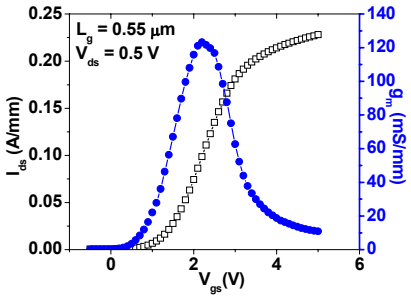

Fig. 8: I_{ds}-V_{gs} and g_m-V_{gs} plot of 0.55µm gate length device at V_{ds} = 0.5V.

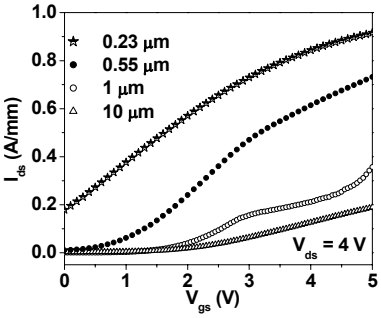

Fig. 9: I_{ds}-V_{gs} plots at V_{ds}= 4 V, for different gate lengths.

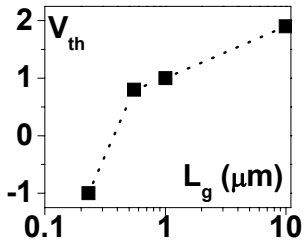

Fig. 10: V_{th} roll off with decreasing gate length.

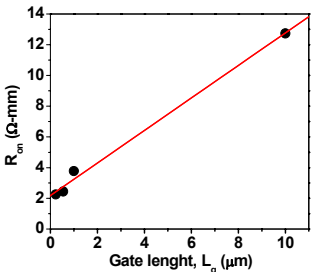

Fig. 11:R_{on} vs L_g plot. A source access resistance of 1Ω-mm is extracted.

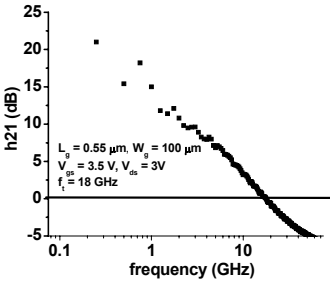

Fig. 12: Small-signal current gain vs. frequency. An extrinsic f_t of 18 GHz is measured.