Anomalous Output Conductance in N-Polar GaN High Electron Mobility Transistors

Man Hoi Wong, *Member, IEEE*, Uttam Singisetti, *Member, IEEE*, Jing Lu, James S. Speck, and Umesh K. Mishra, *Fellow, IEEE*

***Abstract*—An anomalous output conductance that resembled short-channel effects was observed in long-channel N-polar GaN-channel/AlGaN-back-barrier/GaN-buffer high electron mobility transistors. The phenomenon could not be reasonably explained by drain-induced barrier lowering, leakage currents, or impact ionization events. We propose that the output conductance was caused by the ionization of a donorlike hole trap state at the negatively polarized AlGaN-back-barrier/GaN-buffer interface that shifted the threshold voltage at the drain side of the gate, where a high-field depletion region developed beyond current saturation. No evidence of increased output conductance or related device performance degradation was apparent under small-signal high-frequency conditions. The output conductance was suppressed by introducing photogenerated holes that compensated the traps. The effect of several typical back-barrier designs on the dc output conductance was examined.**

***Index Terms*—AlN, back-barrier, GaN, high electron mobility transistors (HEMTs), N-polar, output conductance, polarization, trap.**

I. Introduction

SIGNIFICANT effort has been devoted to establishing the high frequency performance of AlGaN/GaN high electron mobility transistors (HEMTs) to enable high-power microwave and millimeter-wave solid-state power sources. Recent demonstrations of novel techniques and heterostructures such as n^+ contact regrowth and thin Al(In)N barriers with strong polarizations offer device scaling advantages for the next-generation RF and high-speed mixed-signal applications [1]–[9]. As the gate length L_G of the devices decreases to allow for higher frequency of operation, increased confinement of the 2-D electron gas (2DEG) becomes important in reducing short-channel effects (SCEs) such as soft pinchoff and high output conductance under high electric fields. Double heterostructures, such as wide-bandgap buffers [10]–[13] and InGaN back-barriers [9], [14], were commonly employed to reduce current injection into the buffer by raising the conduction-band edge in the buffer with respect to the channel.

Alternatively, N-polar $(000\bar{1})$ GaN-based heterostructures have been proposed as a new epitaxial approach to advance the high frequency performance of GaN HEMTs [15]–[19]. The reversed direction of polarization in N-polar materials compared with the conventional Ga-polar (0001) addresses the challenge of high ohmic contact resistance in GaN-based HEMTs since the 2DEG is induced on top of the wide-bandgap AlGaN barrier. It has been shown that the use of N-polar heterostructures effectively eliminates the bottleneck introduced by the AlGaN barrier in Ga-polar AlGaN/GaN HEMTs to obtaining low contact resistances [20]–[22]. Degenerately-doped InN/InGaN regrown contact layers can be integrated with N-polar HEMTs to fabricate self-aligned transistors with a low contact resistance $< 30\ \Omega \cdot \mu$m [21]. Moreover, N-polar HEMTs have demonstrated large-signal C-band and X-band power performance and cutoff frequencies that compare favorably to state-of-the-art Ga-polar HEMTs [23]–[30]. The high performance of N-polar devices attests the enormous potential of this new technology.

Another major advantage anticipated of N-polar HEMTs is their inherent AlGaN back-barrier for enhanced electron confinement and improved output resistance in scaled GaN HEMTs [31]. Contrary to expectation from simulations and band diagrams, N-polar HEMTs seemed to show increased dc output conductance $G_{\rm DS}$ that led to large threshold voltage (V_T) shifts with increasing drain bias $V_{\rm DS}$ [32], [33]. While this effect resembled drain-induced barrier lowering, high $G_{\rm DS}$ had been observed in N-polar HEMTs with a long L_G and a high aspect ratio, where SCEs were insignificant [34]. In all cases, the off-state leakage was low and could not account for the increase in drain current $I_{\rm DS}$. Moreover, the occurrence of high $G_{\rm DS}$ was independent of the growth technique employed since HEMTs grown by both molecular beam epitaxy (MBE) and metal–organic vapor phase epitaxy (MOVPE) have exhibited high $G_{\rm DS}$ [32], [33], [35]. This paper aims at providing physical understanding and insight into the anomalous $G_{\rm DS}$ in N-polar HEMTs, as well as its implications on device performance and design.

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II. Experiments

A. Role of Impact Ionization

A possible cause of poor current saturation in the field effect transistor (FET) was impact ionization, particularly when the device was operated under semi-on bias conditions due to a combination of sizable electric fields and hot-electron effects [36]. While many researchers considered impact ionization in GaN HEMTs a rare occurrence due to the wide bandgap of the semiconductor [36] and a rapid hot-electron relaxation process via phonon emission [37], electrical and optical signatures of impact ionization in GaN HEMTs have been reported [38], [39]. To determine the extent to which impact ionization might influence the output conductance in N-polar devices, the common-source output characteristics of a well-passivated N-polar HEMT reported in [33] was measured until destructive breakdown. The device was subjected to pulsed measurements to minimize current collapse due to heating using an Agilent 33250A signal generator and a Tektronix TDS 684C oscilloscope. With the device biased at pinchoff on a 50-Ω load line, 200-ns gate pulses at 10% duty cycle were applied. The pulse width was sufficiently long to induce impact ionization events in the high field region at a typical rate of $10^{12}/\mathrm{s}$ by hot electrons traveling at velocities of $1.5 \times 10^7 - 2 \times 10^7$ cm/s [40], [41]. We observed in Fig. 1 that the device showed poor I_{DS} saturation over a wide range of drain biases from the saturation voltage $V_{\mathrm{DS,sat}} \leq 5$ V until destructive breakdown at approximately 60 V. If impact ionization was the cause of the output conductance, then the process of impact ionization would have had to initiate at a low $V_{\mathrm{DS}} \approx V_{\mathrm{DS,sat}}$ and sustain until a much higher $V_{\mathrm{DS}} \approx 60$ V, which was unreasonable considering the avalanche multiplication nature of impact ionization.

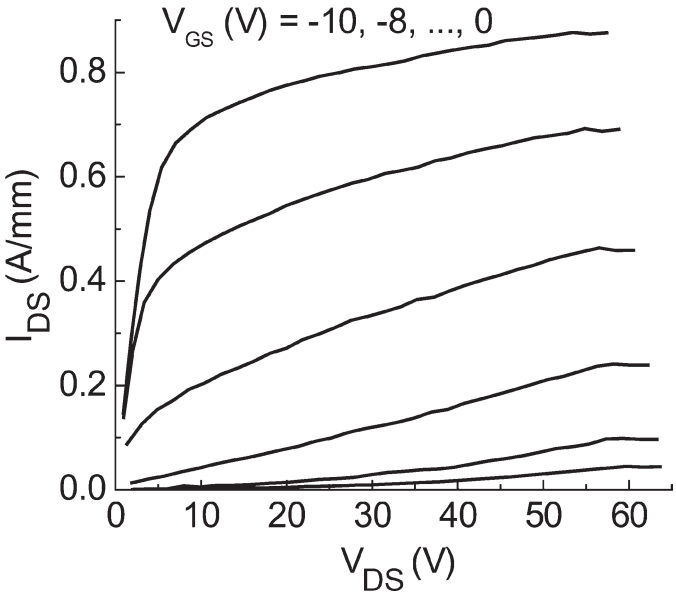

Fig. 1. 200-ns gate-pulsed I–V measurement of a well-passivated N-polar GaN HEMT with an AlN back-barrier [33], showing poor I_{DS} saturation over a wide range of V_{DS}.

B. Device Design and Fabrication

Having ruled out impact ionization as a probable cause for output conductance, we focused this paper on engineering device structures that were guided by a key experimental observation of a hole trap state in III-N heterostructures. For an N-polar GaN/Al_xGa_{1-x}N/GaN heterostructure with $x = 0.3$, the hole trap level E_T was measured by deep-level transient spectroscopy to be at 60 meV from the valence-band edge E_V [42]. The trap was attributed to the net negatively polarized Al_xGa_{1-x}N/GaN interface, in light of a separate work using Ga-polar GaN/InGaN/GaN heterostructures by Schaake who determined that the trap was at the negative GaN/InGaN interface rather than distributed throughout the InGaN [43]. This trap state was known to impact the internal quantum efficiency of III-N light-emitting diodes [43], to cause large-signal dc–RF dispersion in HEMTs [15], [44], to inhibit hole transport or create hysteresis in polarization-induced tunnel junctions [45], [46], and to reduce the efficiency of polarization-assisted acceptor doping [47]. In a nominally undoped N-polar GaN-based HEMT consisting of AlGaN-cap/GaN-channel/AlGaN-back-barrier/GaN-buffer, where the 2DEG was induced at the GaN-channel/AlGaN-back-barrier interface, the equilibrium Fermi level E_F was in close proximity to the hole traps at the negatively polarized AlGaN-back-barrier/GaN-buffer interface (Fig. 2). The accumulation of a 2DEG in the absence of intentional n-type doping suggested the presence of a high density of unintentional donors in the system that could not be accounted for by surface states (since positive surface donors could not compensate the positive polarization charge on an N-polar surface) or unintentional bulk donors (due to their low densities for well-optimized growths) [48], [49]. The hole trap state, considered donorlike due to its charge compensating effect at the negatively polarized interface (NPI) in the sense that it was positive when empty and neutral when occupied, would screen the net fixed polarization charge at the negative interface when ionized without a 2-D hole gas forming and would transfer electrons to the 2DEG channel [15], [45]. Alternatively, a Si δ-doping sheet could be inserted below the AlGaN barrier to supply electrons to the 2DEG channel while the ionized Si donors provided the compensating positive charges, bringing the equilibrium E_F to around midgap near the AlGaN-back-barrier/GaN-buffer interface (see Fig. 2). Two devices with a 30-nm $Al_{0.3}Ga_{0.7}$N back-barrier, one of which was δ-doped with Si (1×10^{13} cm^{-2}) below the back-barrier but was otherwise identical to the other, were designed for the same 2DEG density (see Fig. 3). An $Al_{0.1}Ga_{0.9}$N cap (5 nm) protected the GaN channel layer (25 nm) during the deposition of a 5-nm Si_xN_y gate dielectric by high-temperature chemical vapor deposition (CVD) at 1020 °C prior to fabrication. As will be shown in the following, the position of the equilibrium E_F at the negatively polarized AlGaN-back-barrier/GaN-buffer interface fundamentally determined the occurrence of dc output conductance in long-channel N-polar GaN HEMTs. The negatively polarized AlGaN-cap/GaN-channel interface will not be discussed since its effect, if any, will be reflected in both devices.

The devices were grown by RF plasma-assisted MBE on C-face 6H-SiC substrates. A Ti/Al/Ni/Au (200/1200/300/500 Å) metal stack, annealed at 820 °C for 30 s in N_2, was

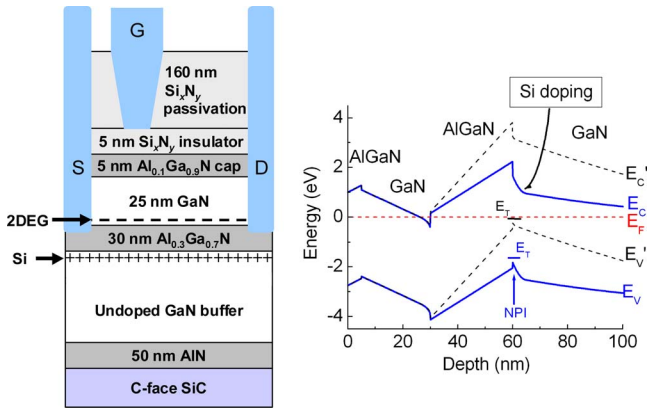

Fig. 2. Layer structure and band diagrams of an undoped (black dashed line) and a Si-doped (blue solid line) N-polar HEMT. The Si-doping prevents the occupancy of the hole trap state (E_T) at the NPI from being modulated by the E_F during transistor operation.

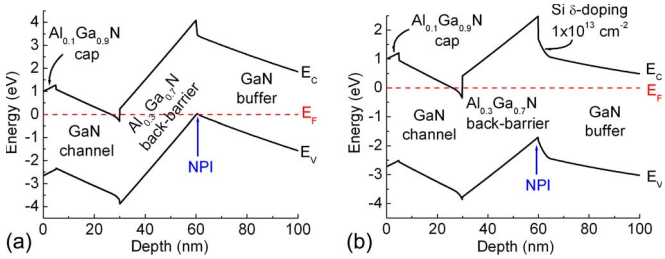

Fig. 3. Device structures of the (a) undoped and (b) Si-doped N-polar GaN HEMTs. The NPI of interest is indicated in each structure.

used as the ohmic contact. Mesas were formed with a BCl_3/Cl_2 reactive-ion etch process. A 160-nm Si_xN_y layer was deposited by plasma-enhanced CVD for surface passivation, followed by a CF_4-based etch of Si_xN_y to form the gate trench with self-aligned Ni/Au/Ni (300/3500/500 Å) gate metal deposition [50]. The devices were 2×75 μm wide with a gate–source spacing $L_{\rm GS}$ of 0.5 μm, a gate–drain spacing L_{GD} of 2 μm, and a nominal L_G of 0.7 μm. Although MBE was the growth technique employed in this paper, we note again that an anomalous output conductance has also been observed in MOVPE-grown N-polar devices [35]. The experiments and discussions that follow make no specific reference to MBE and may be applied to any growth technology without loss of generality.

C. Results and Discussion

1) DC Measurements: Room-temperature Hall measurements showed comparable 2DEG characteristics between the undoped (and doped) devices with a charge density and mobility of 8.4×10^{12} cm^{-2} and 1160 cm^2/V · s (9×10^{12} cm^{-2} and 1100 cm^2/V · s), respectively, which corresponded to sheet resistance values of 630–640 $\Omega/\square$. The dc common-source output characteristics were measured by using an Agilent 4155B semiconductor parameter analyzer. The undoped device showed high $G_{\rm DS}$ with a large $\Delta V_T = -0.45$ V when $V_{\rm DS}$ was increased from 10 to 30 V, whereas the Si-doped device exhibited satisfactory $I_{\rm DS}$ saturation with a much smaller $\Delta V_T = -0.1$ V across the same range of drain biases (see Fig. 4). The undoped device had higher $I_{\rm DS}$ due in part to the V_T shift and

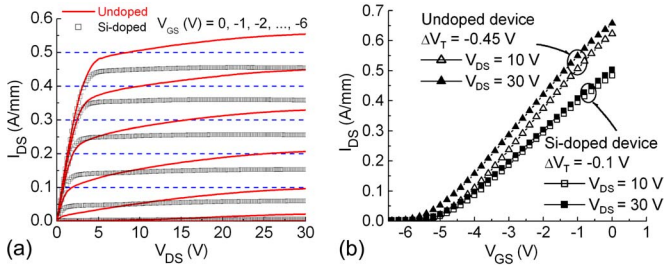

Fig. 4. (a) Common-source output characteristics of the undoped (red line) and Si-doped (black square) N-polar GaN HEMTs. (b) Common-source input characteristics of the undoped and Si-doped N-polar GaN HEMTs.

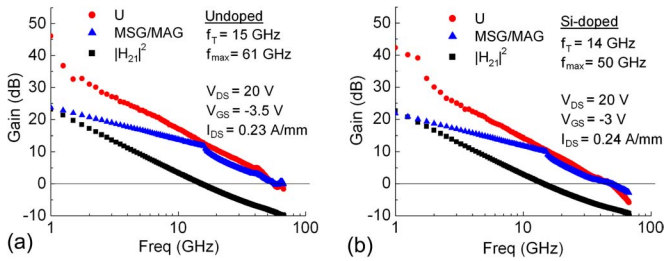

Fig. 5. Small-signal performance of the (a) undoped and (b) Si-doped N-polar GaN HEMTs with pad parasitics de-embedded.

in part to its higher extrinsic transconductance because of its lower contact resistance and slightly higher intrinsic transconductance from process nonuniformities (see Section II-C2). We note that both devices showed low off-state leakage current (< 0.1 mA/mm) at $V_{\rm DS} = 30$ V and that the increase in $I_{\rm DS}$ in the undoped device was reflected in a corresponding increase in the source current. A contrast of the output characteristics and band diagrams between these two devices indicated that an E_F close to E_V (and hence E_T) at the negative AlGaN-back-barrier/GaN-buffer interface resulted in high $G_{\rm DS}$.

2) High Frequency Measurements: To illustrate that a slow trap could be responsible for the high $G_{\rm DS}$, the high frequency performance of the two devices was characterized and compared. Small-signal s-parameter characterization was performed on an Agilent E8361A network analyzer. The unity current-gain cutoff frequency f_T and maximum oscillation frequency $f_{\rm max}$ were obtained by linear extrapolation of the current gain and power gain, respectively, along a 20-dB/dec slope. The small-signal equivalent circuits of the devices were extracted by using on-wafer open–short calibration standards to de-embed the pad parasitics and to extract the intrinsic device parameters [51]. Good agreement between the measured and modeled s-parameters was obtained. The intrinsic RF output resistance $r_{ds,\rm int}$ was evaluated as the reciprocal of the real part of the intrinsic short-circuit output admittance $y_{22,\rm int}$ [52], obtained after further de-embedding the source/drain series resistances that were estimated using transmission-line measurements and optimized during s-parameter modeling. At $V_{\rm DS} = 20$ V, a peak intrinsic $f_{\rm max}$ of 61 GHz was obtained for the undoped device, whereas the Si δ-doped device had a lower peak $f_{\rm max}$ of 50 GHz in spite of its higher dc output resistance (see Fig. 5). We attribute the higher $f_{\rm max}$ of the undoped device to its higher intrinsic transconductance and lower source resistance due to process nonuniformities. The undoped

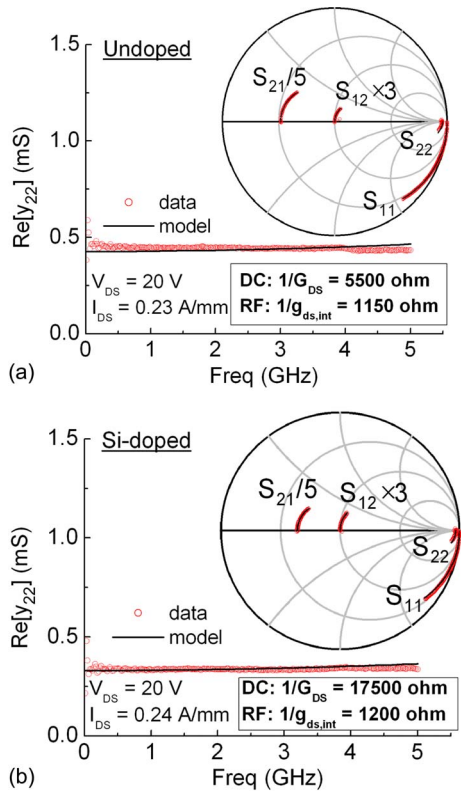

Fig. 6. Measured (red circle) and modeled (black line) s-parameters and $\mathrm{Re}[y_{22}]$ of the (a) undoped and (b) Si-doped devices from 10 MHz to 5 GHz after de-embedding the pad parasitics, showing a good match. The intrinsic output resistance ($r_{ds,\mathrm{int}} = 1/\mathrm{Re}[y_{22,\mathrm{int}}]$; not shown) was obtained by further de-embedding the source/drain series resistances.

TABLE I
COMPARISON OF SMALL SIGNAL EQUIVALENT CIRCUIT PARAMETERS BETWEEN THE UNDOPED AND DOPED HEMTS

	$r_{ds,\mathrm{int}}$ (Ω)	$g_{m,\mathrm{int}}$ (mS)	R_s (Ω)	R_d (Ω)	C_{ds} (fF)	C_{gd} (fF)	C_{gs} (fF)
Undoped	1150	53	19	30	15	13	400
Si-doped	1200	48	31	45	12	16	380

device had therefore suffered no apparent degradation in small-signal high frequency performance, which indicated that the output conductance was strictly a low-frequency phenomenon. In fact, the $r_{ds,\mathrm{int}}$ of the two devices were very comparable at ~1200 Ω, despite their large G_{DS} ratio of 17500/5500 Ω (see Fig. 6 and Table I). These $r_{ds,\mathrm{int}}$ values were in reasonable agreement with the values reported in literature, taking into account their dependence on the gate length and width [53], [54]. The frequency dispersion of $r_{ds,\mathrm{int}}$ could be due to self-heating or bulk/surface trapping effects, which had also been observed in GaAs FETs [55]–[57]. Furthermore, similar $r_{ds,\mathrm{int}}$ values of 1100–1500 Ω were measured in an MBE-grown Ga-polar $Al_{0.3}Ga_{0.7}N$/GaN HEMT of similar dimensions. These results suggested that the high G_{DS} was related to the action of slow traps that were unresponsive to RF signals.

3) Low Temperature Measurements: Further insights were obtained by comparing the room-temperature and low-temperature dc I–V of the undoped device. The low temperature measurements were taken in a cryogenic probe station composed of a wafer stage cooled by liquid nitrogen and a heater to control the temperature. No significant change in G_{DS} was observed when the device was cooled to 100 K (see Fig. 7), which suggested that the physical process that led to poor drain current saturation was not thermally activated but should be instead driven by electrostatics when the device was under dc bias.

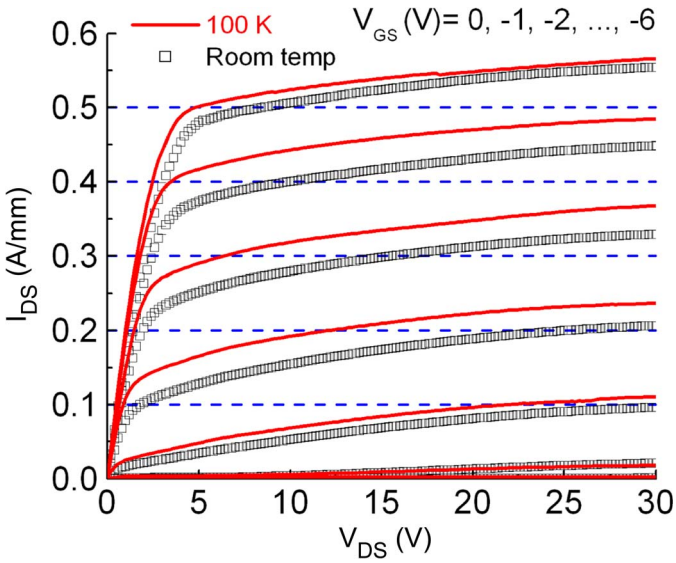

Fig. 7. DC I–V at room temperature (black square) and 100 K (red line) of the undoped HEMT showing no significant difference in output conductance.

4) Suppression of Output Conductance With Holes: The temperature insensitivity of the G_{DS} was expected if the G_{DS} was related to the near-valence-band donorlike hole trap. As the traps that remained unionized were capable of capturing holes, we anticipated recovering high output resistance in the undoped device if these traps could be compensated with holes. However, the intrinsic hole concentration due to thermal generation in the wide-bandgap ($>$ 3.4 eV) (Al)GaN material system was insignificant. High hole concentrations could be obtained through either p-type doping or photogeneration to create electron–hole pairs. Grundmann achieved efficient tunneling in Ga-polar p-GaN/AlN/n-GaN tunnel junctions by using modulation p-doping to compensate the hole traps at the negatively polarized p-GaN/AlN interface [45]. In our experiment, a broadband UV light source (EXFO OmniCure S1000 spot curing system) with a power density of 18 mW/cm^2 and a wavelength down to 280 nm, which was capable of optical excitation across the bandgap of the $Al_{0.3}Ga_{0.7}N$ back-barrier, was used to illuminate the undoped device. The device was first illuminated for 3 min with no external bias applied to achieve a steady state. Under continued illumination, it was then subjected to a gate-pulsed I–V measurement to minimize any effect of device heating, as described in Section II-A. The holes generated by the UV light were collected at the negative AlGaN-back-barrier/GaN-buffer interface where a potential well for holes existed to compensate the traps. As a result, the illuminated undoped device showed an order-of-magnitude reduction in G_{DS} at $(V_{\mathrm{DS}}, V_{\mathrm{GS}}) = (15\ \mathrm{V},\ 0\ \mathrm{V})$, compared with its unilluminated dc output I–V (see Fig. 8). The insignificant change in G_{DS} at low drain biases beyond the $V_{\mathrm{DS,sat}}$ suggested incomplete compensation of the traps

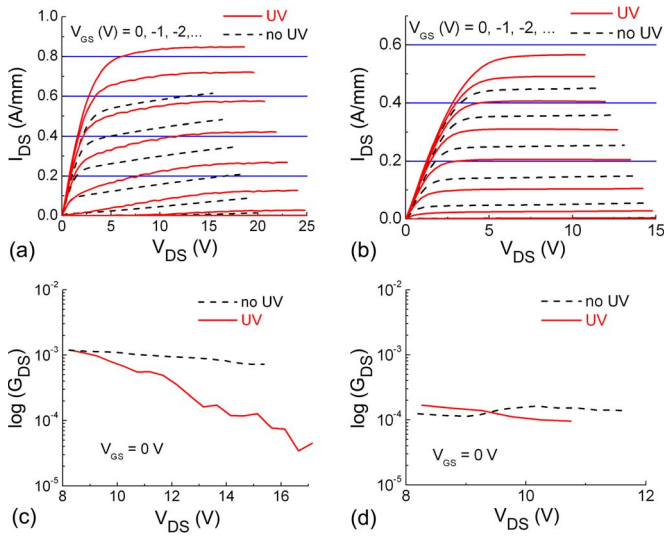

Fig. 8. Room-temperature common-source output characteristics of the (a) undoped and (b) Si-doped HEMTs without (black dotted line) and with (red solid line) UV exposure, as well as the $G_{\rm DS}$ of the (c) undoped and (d) Si-doped HEMTs at $V_{\rm GS} = 0$ V without (black dotted line) and with (red solid line) UV exposure.

in the steady state that, considering the donorlike nature of the traps, could cause high $G_{\rm DS}$ with increasing $V_{\rm DS}$ via an ionization process under the increasing electric field. Further increase in $V_{\rm DS}$ led to a fast decrease in $G_{\rm DS}$ when most traps were either compensated or ionized. For comparison, the doped device showed no significant change in $G_{\rm DS}$ with UV illumination, as expected from its high unilluminated dc output resistance (see Fig. 8). The photogenerated carriers contributed to increased 2DEG density in both devices that resulted in lower on-resistances, higher $I_{\rm DS}$, and shifted V_T, all of which were inconsequential to interpreting the behavior of $G_{\rm DS}$.

III. Proposed Physical Model of Output Conductance

The four sets of experimental results presented thus far have collectively shown that the anomalous $G_{\rm DS}$ in N-polar GaN HEMTs originated from a slow-responding hole trap at the negatively polarized AlGaN-back-barrier/GaN-buffer interface, based on which we propose a physical mechanism to explain the phenomenon.

The absence of Si-doping below the AlGaN back-barrier in an N-polar HEMT brought the equilibrium E_F in close proximity to the donorlike hole trap state, as suggested by the band diagram in Fig. 2. As the $V_{\rm DS}$ was increased beyond the $V_{\rm DS,sat}$ at a given *fixed* $V_{\rm GS}$ under dc conditions, a depletion region was formed on the drain side of the gate where the donorlike traps were ionized, and electrons were transferred to the high field region of the 2DEG channel. The resultant positive charge in the traps caused a negative shift in the threshold voltage at the drain side of the gate. A higher $V_{\rm DS}$ was therefore needed to reestablish $I_{\rm DS}$ saturation as $V_{\rm DS,sat} = V_{\rm GS} - V_{T(\text{drain side of gate})}$ in the simplest approximation, causing more traps to be ionized to further shift the $V_{\rm DS,sat}$ toward an even higher drain bias. This process reiterated such that the $I_{\rm DS}$ continuously increased with $V_{\rm DS}$ until the device destructively broke down. The Si-doping could suppress this process by separating the trap level from the E_F to prevent the change in the occupancy and hence the charge state of the traps. However, our experiments could not rule out the possibility that the Si-doping increased the formation energy of the hole traps so that these traps were actually absent in that device. As for the pulsed I–V measurements employed in this paper, the device was biased at pinchoff as the $V_{\rm DS}$ was increased in discrete steps. A series of gate voltage pulses were applied to the device following each $V_{\rm DS}$ step. For each $V_{\rm DS}$ increment, the $V_{T(\text{drain side of gate})}$ was shifted according to the mechanism described above, causing the output conductance under pulsed conditions.

While the hole trap state was considered to be responsible for the increase in $I_{\rm DS}$, dc–RF dispersion or current collapse in N-polar GaN HEMTs had also been attributed to the same hole trap state [15]. This apparent contradiction could be resolved by recognizing that the $V_{\rm GS}$ instead of $V_{\rm DS}$ was the variable voltage in the mechanism causing current collapse and that the traps involved in current collapse were located under the gate instead of at the drain side of the gate. In [15], the 2DEG under the gate was modulated with the application of a negative $V_{\rm GS}$ until the device was pinched off at $V_{\rm GS} = V_{T(\text{under gate})}$, where $V_{T(\text{under gate})}$ was the threshold voltage under the gate. The concentration of the ionized hole traps under the gate remained unchanged for $|V_{\rm GS}| < |V_{T(\text{under gate})}|$ since the 2DEG screened the negatively polarized AlGaN-back-barrier/GaN-buffer interface from the gate bias. As $|V_{\rm GS}| > |V_{T(\text{under gate})}|$, the hole traps under the gate were no longer screened, and more traps were ionized to image the negative charges at the gate electrode. These additional hole traps that were ionized but did not contribute to the 2DEG charge would cause dc–RF dispersion since they needed time to recapture electrons before the 2DEG channel could be reestablished with $|V_{\rm GS}| < |V_{T(\text{under gate})}|$. A more detailed discussion of this process is available in [15].

IV. Output Conductance in Advanced N-Polar Device Structures

A. Graded-AlGaN Back-Barrier HEMT

Rajan *et al.* had first proposed a methodology to eliminate dc–RF dispersion in N-polar GaN HEMTs by grading the AlGaN-back-barrier/GaN-buffer interface, where ionized Si donors were used to maintain an equilibrium E_F above midgap throughout the graded-AlGaN layer by compensating the negative space charge ρ induced by the gradient in polarization $\overline{P}$, according to the relationship $\rho = -\nabla \cdot \overline{P}$ [15]. Following their design principle, we fabricated a device with an $Al_xGa_{1-x}N$ back-barrier linearly-graded in x from 0.05 to 0.3 with a uniform Si doping concentration of 4.5×10^{18} cm^{-3}, followed by a 5-nm undoped $Al_{0.3}Ga_{0.7}N$ spacer (see Fig. 9). The HEMT had a 2DEG density and mobility of 9.7×10^{12} cm^{-2} and 820 cm^2/V · s, respectively. This device structure could be viewed as a variation of the Si δ-doped structure described above by spreading the negative polarization sheet charge at the AlGaN-back-barrier/GaN-buffer interface into a 3-D space charge, as well as distributing the δ dopant sheet as bulk doping

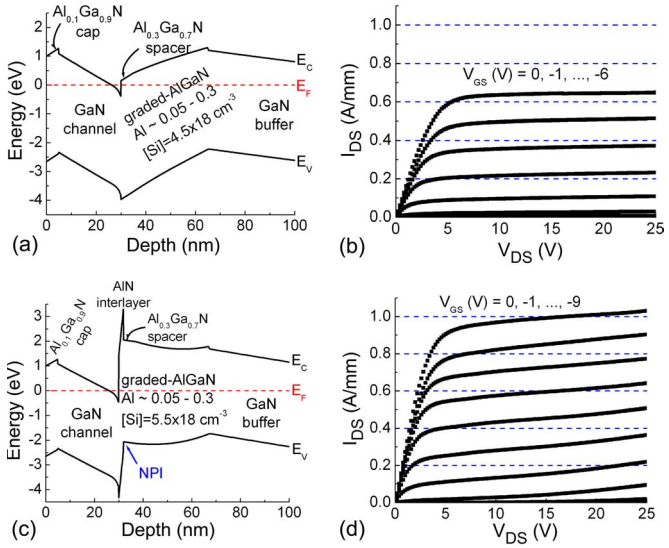

Fig. 9. (a) Band diagram and (b) dc I–V of the graded-AlGaN back-barrier HEMT without an AlN interlayer. (c) Band diagram and (d) dc I–V of the graded-AlGaN back-barrier HEMT with an AlN interlayer, where the NPI of interest is indicated in (c).

throughout the graded-AlGaN layer. We therefore expected and indeed measured a high dc output resistance through its common-source output characteristics (see Fig. 9).

B. Graded-AlGaN Back-Barrier HEMT With an AlN Interlayer

An effective method of improving the 2DEG mobility in III-N HEMTs is by inserting a thin AlN interlayer between the GaN channel layer and the AlGaN spacer layer to reduce alloy scattering [58]. In an N-polar device structure, the AlN interlayer creates a NPI with the underlying AlGaN back-barrier, where hole traps could form. To examine the impact of the negatively polarized AlN/AlGaN interface on $G_{\rm DS}$, we added a 2-nm AlN interlayer to the graded-AlGaN back-barrier device described in Section IV-A. Due to the additional negative polarity of the AlN/$Al_{0.3}Ga_{0.7}N$ interface, a higher Si doping of 5.5×10^{18} cm^{-3} was needed to maintain a midgap equilibrium E_F throughout the graded-AlGaN layer and near the AlN/$Al_{0.3}Ga_{0.7}N$ interface (see Fig. 9). As a result, this device had a higher 2DEG density of 1.4×10^{13} cm^{-2} and an improved mobility of 1230 cm^2/V $\cdot$ s. Despite the large energy separation between the E_V and the equilibrium E_F, the device with an AlN interlayer clearly exhibited higher $G_{\rm DS}$ than the interlayer-free structure (see Fig. 9). This result could be attributed to the action of a hole trap at the negatively polarized AlN/$Al_{0.3}Ga_{0.7}N$ interface, where the trap state might be deeper in the bandgap than the 60-meV level measured for an $Al_{0.3}Ga_{0.7}N$/GaN interface.

It is conceivable that the trap concentration and/or energy might depend on the bandgap of the materials or the net negative polarization charge density at the interface. The bandgap effect could be overcome by engineering the Si dopant profile, whereas the interfacial charge density could be reduced by increasing the Al content of the underlying spacer layer. However, grading the AlGaN barrier to AlN would necessitate simultaneous implementation of epitaxial strain management techniques to prevent strain relaxation. Alternatively, InAlN back-barriers that are lattice-matched to GaN provide another plausible solution. Further studies are needed to evaluate the effectiveness of the various strategies.

V. Conclusion

The origin and behavior of the anomalous $G_{\rm DS}$ in N-polar GaN HEMTs have been investigated using four device structures with systematic changes in the back-barrier design: 1) an undoped AlGaN back-barrier; 2) an AlGaN back-barrier with backside Si δ-doping; 3) a graded-AlGaN back-barrier uniformly-doped with Si; and 4) a Si-doped graded-AlGaN back-barrier with an mobility-enhancing AlN interlayer. We propose that the $G_{\rm DS}$ was caused by the electrostatics of a donorlike hole trap state at a negatively polarized AlGaN-back-barrier/GaN-buffer or AlN-interlayer/AlGaN-back-barrier interface below the 2DEG. It was a dc or low-frequency phenomenon resembling the SCE that shifted the V_T of the device at the drain side of the gate with $V_{\rm DS}$, whereas no evidence of increased output conductance or related device performance degradation was found under RF ($>$ 100 MHz) conditions for high-speed applications. The dc output conductance in N-polar GaN HEMTs could be eliminated by appropriate back-barrier designs such as in the second and third structures described above, with the key criterion being a midgap placement of the E_F in the vicinity of a NPI, such that the hole trap state near the valence band remains filled and neutral.

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