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Letter

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Conduction Mechanisms in CVD-Grown Monolayer MoS_2 Transistors: From Variable-Range Hopping to Velocity Saturation

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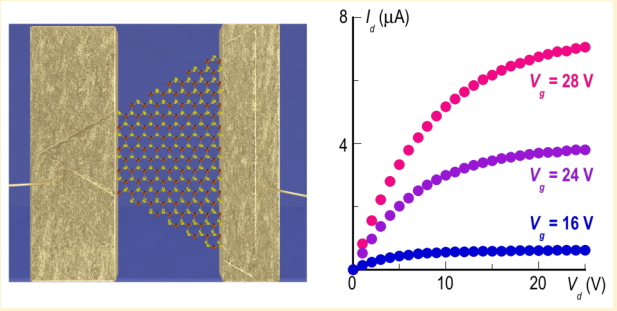
S *Supporting Information*

ABSTRACT: We fabricate transistors from chemical vapor deposition-grown monolayer MoS_2 crystals and demonstrate excellent current saturation at large drain voltages (V_d). The low-field characteristics of these devices indicate that the electron mobility is likely limited by scattering from charged impurities. The current−voltage characteristics exhibit variable range hopping at low V_d and evidence of velocity saturation at higher V_d. This work confirms the excellent potential of MoS_2 as a possible channel-replacement material and highlights the role of multiple transport phenomena in governing its transistor action.



KEYWORDS: *Molybdenum disulfide, transition metal dichalcogenides, 2D transistors, high-field transport, velocity saturation*

Transition-metal dichalcogenides have recently emerged as a new class of electronic materials, which, much like graphene, may be isolated in a two-dimensional (2D) form to implement a variety of novel electronic devices.[1] Among the materials that comprise this group, molybdenum disulfide (MoS_2) is one whose characteristics appear particularly promising for such applications. In marked contrast to graphene, MoS_2 exhibits a large energy gap (1.3−1.8 eV), the direct nature of which in the monolayer form makes it attractive for not only transistor implementations but also optoelectronics. Efficient transistor action has been demonstrated for devices based on multilayer and monolayer MoS_2,[1−23] and these devices are characterized by large ($>10^7$) room-temperature ON-OFF ratios. They are also predicted to exhibit excellent subthreshold swing and benefit from immunity to short-channel effects.[24] Although the large effective mass ($m^* = 0.45m_o$) of the MoS_2 electrons means that they exhibit much lower mobility than the massless Fermions of graphene, this is not expected to be problematic for many applications involving transistor switching. In one pioneering study, MoS_2 transistors were used to implement small-scale integrated circuits,[25] providing essential Boolean functionality. Other work has demonstrated their application as sensitive photodetectors[26,27] capable of operating in the visible and UV ranges. Additionally, and in common with graphene, the ability to exploit valley polarization as a state variable in (monolayer) MoS_2 may open up the development of new "valleytronic" devices.[28−30]

In the vast majority of studies reported in the literature to date, MoS_2 transistors have been fabricated by mechanically exfoliating 2D material onto an insulating substrate from crystalline molybdenite.[2−9,13−18,20,22,23,25,26] Although this has the benefit of allowing rapid prototyping of individual devices, chemical routes to synthesis[10−12,19,21,31−33] offer the prospect of both high material yield and uniformity. Chemical vapor deposition (CVD), involving the sulfurization of molybdenum films deposited on Si/SiO_2 substrates, is one such promising approach.[11,12,19,31,32] Depending on the initial film thickness a variety of final structures can be realized, including monolayer crystals with areas of many tens of square microns. These structures may then easily be subjected to in situ device fabrication or may be released into solution for transfer to other substrates.[19] Structural characterization (via Raman spectroscopy and atomic-force microscopy) of the CVD-grown crystals confirms their monolayer,[11,12] highly crystalline[33] character, making this approach particularly attractive for transistor realization. Recently, there have been some reports[11,12,19] of the electrical characteristics of such devices, suggesting that they are able to compete with or even exceed the performance offered by their exfoliated counterparts. In ref 21, the authors presented a detailed study of the influence of thermal annealing

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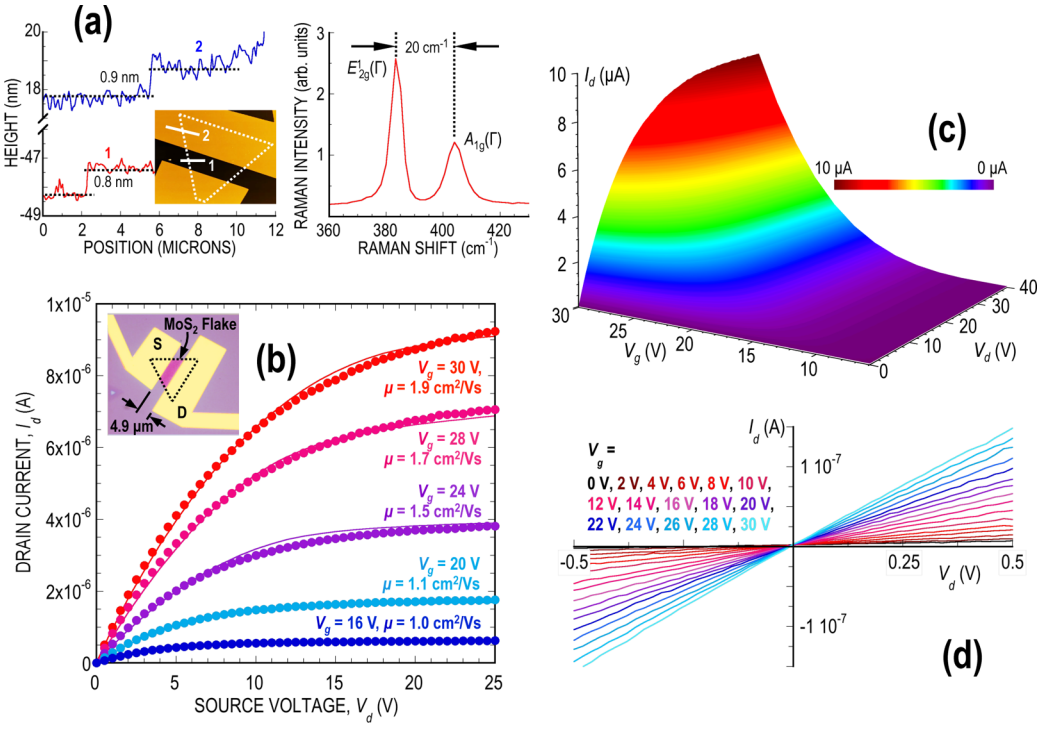

Figure 1. (a) Shown on the left are line scans recorded along the two white solid lines in the AFM image shown in the inset. The image is of MS2-13, and the outline of the MoS_2 crystal is indicated by the white dotted line. The figure on the right is a Raman spectrum obtained using a (514.5 nm wavelength, 1 μm spot size) laser to illuminate the channel of MS2-13. (b) Transistor curves measured at room temperature for transistor MS2-13 (shown in the false-color optical micrograph in the inset). Filled symbols are experimental data points, and solid lines represent the results of simulations (see main text for details). (c) Color contour plot showing the full evolution of $I_d(V_d, V_g)$ for device MS2-13. (d) Expanded view of the transistor curves around $V_d = 0$, showing the linearity of the current over the full range of V_g.

on the transistor characteristics and showed that this allowed low-temperature (10 K) mobility values as large as 500 cm^2 V^{-1} s^{-1}) to be obtained. Moreover, the authors were able to demonstrate evidence of a metal−insulator transition as a function of gate voltage, suggestive of the high electronic quality of the CVD-grown crystals.

In this Letter, we present the results of studies of the electrical properties of transistors implemented in CVD-grown, monolayer MoS_2. We demonstrate, for the first time, excellent current saturation in such devices and explore the role of different transport mechanisms in governing the dependence of their drain current (I_d) on the drain (V_d) and gate (V_g) voltages. For drain voltages in the linear regime, we observe clear signatures of variable-range hopping (VRH) in the temperature (T)-dependent conduction, reminiscent of prior studies of exfoliated MoS_2.[3,13] The VRH weakens with an increase in the gate voltage, presumably as electrons in the channel are able to more effectively screen out the impurity-related background potential. This behavior is accompanied at higher fields by the emergence of velocity saturation. The need to introduce the latter phenomenon arises from the strongly gate-voltage dependent character of the channel mobility (μ), and the saturation velocity ($v_{sat} = 3 \times 10^6$ cm s^{-1}) used to fit the experiment is found to closely match that reported in recent studies of multilayer MoS_2.[34] Simulations of the electrostatics within the device confirm that the velocity saturation arises from the presence of a strongly peaked electric field (E_y, where y is the direction along the channel length), which develops in the channel near the drain contact under current saturation.

Monolayer MoS_2 transistors were fabricated using electron-beam lithography and metal lift-off to form Cr/Au (5 nm/50 nm) source-drain contacts to CVD-grown single MoS_2 crystals synthesized on commercial Si/SiO_2 wafers. The heavily doped Si served as the back-gate of the transistor, whereas the 280 nm thick SiO_2 functioned as the gate dielectric and was also used to provide optical contrast when observing the MoS_2 crystals under an optical microscope. (In the ultimate applications, this design could be replaced with one consisting of a top gate formed on a thin layer of high-k dielectric, significantly lowering the working gate-voltage range while also enhancing the mobility through "engineering" of the dielectric environment.[2]) The CVD growth was performed by first dispersing MoO_3 nanoribbons onto the Si/SiO_2 substrate and then sulfurizing them in a furnace.[32] This process resulted in the formation of triangular-shaped single crystals, 13 ± 2.5 μm on a side, whose monolayer character was confirmed by both Raman studies and atomic-force microscopy. This is indicated in Figure 1(a), in which the measured thickness of the MoS_2 crystal and the separation of the E^1_{2g} (Γ) and $A_{1g}(\Gamma)$ Raman peaks are both consistent with earlier reports for CVD grown monolayer MoS_2.[11,21]

The electrical characteristics of 13 different transistors were investigated for this study and were all found to exhibit fairly similar characteristics (see Table 1 of the Supporting Information, where we also define the notation used to identify the different transistors). For this reason, in our discussions here we focus on providing the results of a comprehensive study of a single device (MS2-13), which we have chosen due to its representative character. This device is shown as an inset in Figure 1(b), where the source (S) and drain (D) contacts are indicated. After fabrication, transistors were wirebonded into standard DIP packages and mounted in a cryostat, allowing

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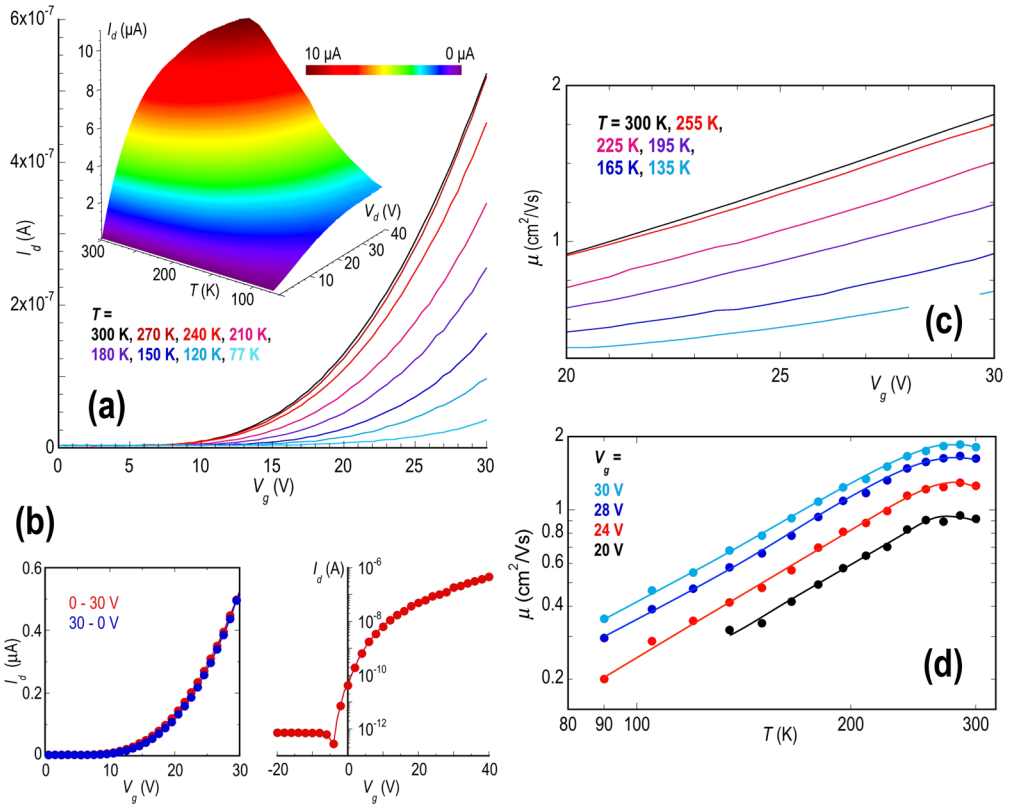

Figure 2. (a) Transfer characteristics of device MS2-13 (V_d = 0.5 V), measured at various temperatures from 77 to 300 K. The inset plots the variation of $I_d(V_d)$ as a function of temperature from 77 to 300 K. The gate voltage (V_g = 30 V) was held fixed for these measurements. (b) The left panel shows the transfer curve of MS2-13 measured at 300 K in both sweep directions (red and blue data). In the right panel, we use a semilog plot to reveal an on−off ratio at 300 K of ∼6 orders of magnitude. The measurement was made with V_d = 1 V using a Keithley 4200 with a high resolution preamplifier. (c) Variation of mobility as a function of V_g, inferred (using eq 2) from the experimental data of (a) at different temperatures. (d) Variation of mobility as a function of temperature, inferred from the results of (c) at various gate voltages. The solid lines are trend lines that form a guide to the eye.

their electrical characteristics to be measured from 77 to 300 K with a Keithley 2400 source meter. The measurements reported here were obtained with the samples maintained under vacuum, in the dark, and in the absence of any annealing.[15,21] We have performed both in situ (under vacuum, 110 °C, 10^{-5} mbar, 20 h) and ex situ (also under vacuum, 120 °C, 10^{-5} mbar, 20 h) annealing of our devices, but in contrast to earlier reports,[15,21] do not find such a significant improvement in performance. The key features of transistor action (including the well-defined current saturation that we show below) are preserved after annealing, and current levels are increased by ∼50%, but this improvement is much less dramatic than that achieved in refs 15 and 21. The reasons for this are unclear at present and require further investigation.

In Figure 1(b) and (c), we show measurements of the transistor curves of device MS2-13 at room temperature. Figure 1(b) shows the characteristics measured at several discrete gate voltages, along with corresponding theoretical fits (solid lines), whose details are provided further below. Figure 1(c) is a color contour that expresses the evolution of I_d as a continuous function of V_d and V_g. Both figures reveal classic transistor action with excellent saturation at high drain voltages, something that has not been demonstrated for CVD-grown MoS_2 devices (for which previous works have focused primarily on analyzing the transfer characteristics[11,12,15,19,21]). In Figure 1(d), we confirm the linear character of the current for small V_d and for a wide range of V_g. Typically, such linearity in two-terminal measurements is taken to indicate that good ohmic contact has been achieved to the MoS_2 channel.[21]

In the main panel of Figure 2(a), we present measurements of the transfer (I_d−V_g) characteristic of transistor MS2-13 at a series of temperatures from 77 to 300 K. As indicated in Figure 2(b), the transfer curve showed little hysteresis as a function of sweep direction (left panel), and yielded a room-temperature on−off ratio of ∼6 orders of magnitude (right panel). Regardless of the temperature in Figure 2(a), it is noted that none of the curves show the linear variation $I_d(V_g)$ expected from a simple square-law model[35]

$$I_d = \frac{W\mu}{L}\frac{\varepsilon_{ox}\varepsilon_o}{x_o}\left[(V_g - V_T)V_d - \frac{V_d^2}{2}\right] \quad (1)$$

Here, V_T is the threshold voltage, L is the channel length, x_o is the oxide thickness, and ε_{ox} is its dielectric constant. W is the channel width, which in this work is taken as the average width of the MoS_2 crystal at the source and drain ends. μ is an effective channel mobility and, when this parameter is independent of gate voltage, its value can be determined from the linear relation between the drain current and the gate voltage [i.e., $\mu = (dI_d/dV_g)(x_o/(\varepsilon_{ox}\ \varepsilon_o))(L/WV_d)$]. The nonlinearity of the curves in Figure 2(a) indicates that the mobility in these devices is gate-voltage dependent however, requiring us to determine μ by solving the following expression (for details see the Supporting Information).

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$$\mu + (V_g - V_T)\frac{d\mu}{dV_g} = \frac{L}{W}\frac{x_o}{\varepsilon_{ox}\varepsilon_o}\frac{1}{V_d}\frac{dI_d}{dV_g} \quad (2)$$

In Figure 2(c), we plot the variation of $\mu(V_g)$ determined from the experimental transfer curves at various temperatures using eq 2. The mobility clearly increases in an almost linear manner with increasing V_g and is also systematically larger at higher temperatures. This latter point can be seen explicitly in Figure 2(d), where we plot the variation of $\mu(T)$ at four different values of V_g. The behavior here is similar to that found previously for exfoliated MoS_2[17] and is consistent with the role of charged-impurity scattering.[1,5] The temperature dependence of the mobility is reflected as a strong variation of the transistor curves, as we indicate in the inset to Figure 2(a). This color contour plots the I_d–V_d characteristic of transistor MS2-13 at fixed gate voltage and at a series of different temperatures. As the mobility increases with temperature, the overall current level exhibits significant growth. At every temperature, however, we observe clear signatures of the linear- and saturated-current regimes, indicating that the transistor action is robust.

Turning to the issue of the conduction mechanism in the MoS_2 transistors, this is strongly dependent upon both the drain and gate voltages. For small V_d, we observe clear signatures of 2D VRH in the resistance[3,13]

$$R \propto R_o \exp\left[\left(\frac{T_o}{T}\right)^{1/3}\right] \quad (3)$$

where R_o and T_o are appropriate fit parameters. In Figure 3(a), we show the variation of the resistance (R) as a function $T^{-1/3}$ (on a semilog plot) and obtain good agreement with the VRH form for a wide range of gate voltages. The resistance values plotted here were determined at V_d = 1 V, well within the linear regime of transistor operation. In Figure 3(b), we plot the variation of T_o, inferred from the data of Figure 3(a), as a function of the gate voltage. Clearly, there is a trend for T_o to decrease with an increase in V_g, indicating that the role of the VRH is correspondingly reduced. We have already noted that the increase in mobility that we observe upon increasing temperature is indicative of the role of strong charged-impurity scattering. The related observation of VRH suggests that these charged impurities, which are presumably associated with the substrate,[3] also give rise to the disordered potential landscape needed for hopping to dominate. As the carrier concentration is increased by raising the gate voltage, screening of the impurity potential should then suppress the role of the hopping. MoS_2, like graphene, is known to be characterized by inefficient screening, particularly when prepared in few-layer form.[36−39] Estimates for the screening length vary, dependent upon the number of layers, but are typically in the range of several nanometers.[36−39] Screening of the impurity potential will therefore be incomplete in the devices, but we nonetheless expect that it should improve as the carrier concentration increases.[40] From our SILVACO simulations described in further detail below, we find that an increase in the gate voltage from 16 to 30 V should raise the carrier concentration in the MoS_2 from 0.4×10^{12} to 2.2×10^{12} cm^{-2}. According to recent theoretical work,[40] the increased density should lead to improved screening, and it is this phenomenon that we suggest is responsible for the modest improvements in mobility achieved in Figure 2(c).

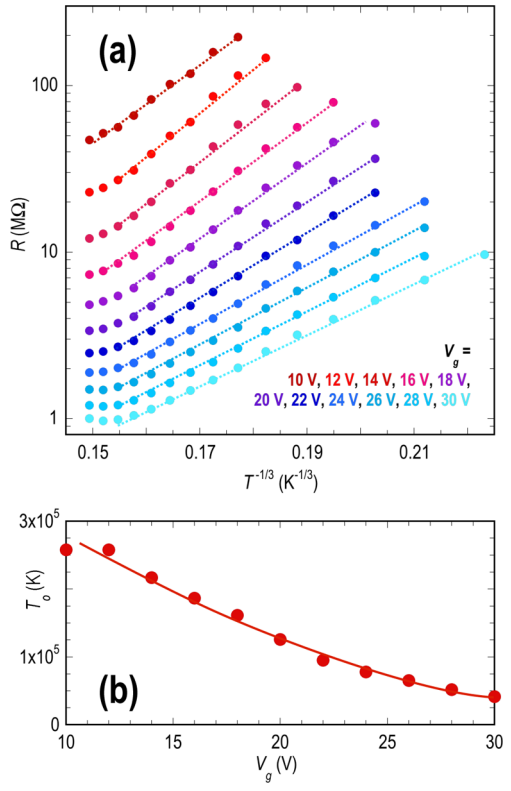

Figure 3. (a) Temperature-dependent variation in the resistance of device MS2-13 plotted to reveal the connection to VRH. A source voltage of V_d = 1 V was used for these measurements. (b) Gate-voltage-dependent variation of the VRH parameter T_o (see eq 3).

For a more quantitative understanding of transistor action, we have simulated the performance of the devices using the SILVACO Atlas package.[41] Details of the calculations are provided in the Supporting Information, along with a full list of the material parameters used. The essential idea, however, is that the monolayer MoS_2 crystal is treated as a 0.5 nm thick film, and a classical drift-diffusion model is used to simulate the drain current. The calculations explicitly consider the triangular shape of the MoS_2, and use micrographs of the actual device to determine the orientation of the crystal relative to the contacts. To account for the influence of velocity saturation, a field-dependent mobility ($\mu(E_y)$) is used, such that

$$\mu(E_y) = \mu_o\left[\frac{1}{1 + (\mu_o E_y/v_{sat})^\beta}\right]^{1/\beta} \quad (4)$$

where E_y is the electric field along the direction of current flow. Because the conduction in these devices is dominated by electrons, we take the parameter β = 2.[42] The low-field mobility (μ_o) in eq 4 is then determined by fitting the drain current to match that obtained in the linear region of the transistor curves.

Using the approach described above, we are able to successfully reproduce the experimental transistor curves of Figure 1(b). In doing so, we infer low-field mobility values in good agreement with those determined from the experimental data. This is illustrated in the inset to Figure 4(b), where we plot as discrete points the mobility values used in our simulations and compare them with those determined experimentally at room temperature. The agreement between the simulation and experiment is good, being within the error bars associated with the former. (The error bars reflect

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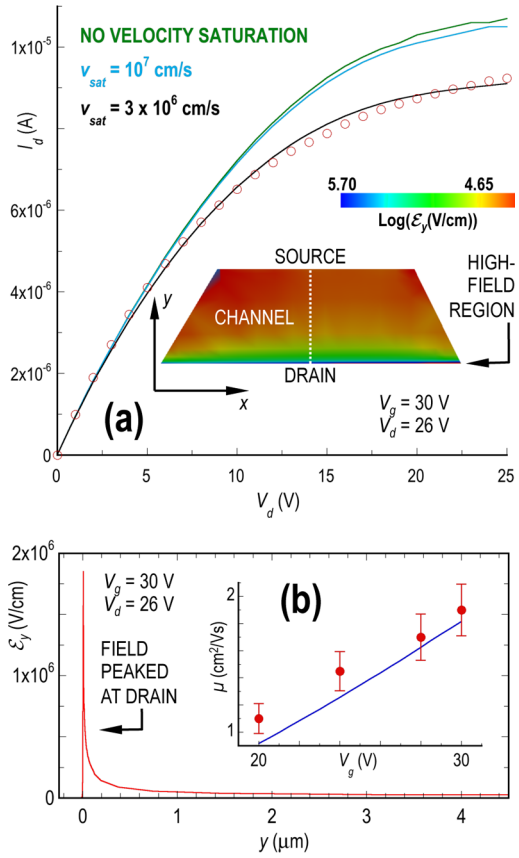

Figure 4. (a) Simulated fits to the drain current (V_g = 30 V), using different values for v_{sat} (indicated). A saturated velocity of 3 × 10^6 cm s^{-1} is found to best fit the experimental data (open symbols). The inset plots the calculated electric field strength (E_y) as a function of position within the channel (for V_g = 30 V, V_d = 26 V). The field strength is plotted on a log scale here (see color bar) and is strongly peaked at the drain end. (b) Variation of E_y as a function of position along the center line of the channel, indicated by the white dotted line. y = 0 corresponds to the drain end of the device. V_g = 30 V; V_d = 26 V. (inset) Comparison of experimentally determined mobility at 300 K with that used in the simulations to match the transistor curves. Device MS2-13. Solid line: experimental data. Filled symbols: simulated mobility values.

primarily the variation that arises when computing the mobility using the width of the triangular channel at its source and drain ends. The data points themselves were obtained by using an averaged valued for this width.)

An important feature revealed by our simulations is that current saturation at large V_d results from an interplay between channel pinch-off at the drain end and velocity saturation of electrons in the channel. At low gate voltages, where the mobility is small, the current saturation results primarily from pinch-off, whereas the converse is true at higher gate voltages. Referring to the transistor curves of Figure 1, for example, for gate voltages lower than 25 V, our simulations show that the drain current is generally consistent with a simple square-law model without the need for any velocity saturation. For larger gate voltages, however, agreement with the experiment is only possible by properly accounting for velocity saturation. This can be seen in Figure 4(a), where we show how the choice of different values for v_{sat} influences the computed current. The experimental data are plotted as open symbols in the figure, and it is clear that, with no velocity saturation (green line) or with an assumed v_{sat} = 10^7 cm s^{-1} (blue line), the simulated current is significantly larger than the experimental current. With v_{sat} = 3 × 10^6 cm s^{-1}, a value suggested in previous work on multilayer MoS_2 transistors,[34] however, the agreement is very good. In the inset to Figure 4(a), we plot a 2D surface contour of the channel field (E_y) using a logarithmic scale. The figure reveals that the velocity saturation is due to the strongly peaked nature of this field near the drain, a feature that can also be seen in Figure 4(b). Here, we plot the variation of E_y as a function of position (y) along the center line indicated by the white dotted line in the color contour of Figure 4(a). The field at the drain end approaches 2 × 10^6 V cm^{-1}, from which value and the mobility of 1.9 cm^2 V^{-1} s^{-1}, we obtain an estimate for the saturated velocity of 3.8 × 10^6 cm s^{-1}. This is consistent with our discussion above regarding the influence of the velocity saturation on the drain current in Figure 4(a).

The mobility values determined here (∼1−10 cm^2 V^{-1} s^{-1}, see Table 1 in the Supporting Information) are, in many cases, much lower than those reported elsewhere. Putting aside the fact that the estimates provided in many of these studies have been called into question by others,[43] there are three primary issues that are likely at play here. First, our measurements are performed on unannealed devices, whereas thermal annealing has been demonstrated to provide improvements in the mobility.[15,21] Second, and perhaps more importantly, our work here shows that the mobility is strongly gate-voltage dependent, such that further increasing the gate voltage beyond the threshold can be expected to result in larger mobility values. In ref 21, for example, room-temperature mobility as large as 50−60 cm^2 V^{-1} s^{-1} was reported but was achieved by using back-gate voltages approaching 100 V. Finally, our two-terminal measurements may be influenced by contact resistance, which would result in an underestimate of the mobility. Although contact resistance was not included in the simulations shown in Figure 4, we have performed calculations in which the source/drain contact resistance was increased up to 1 kΩ (inclusion of larger values than this introduces problems with convergence) and did not observe any significant change in drain current. This can be attributed to the much lower conductance of the FET channel itself.

It is informative to compare the results of our study with those found in similar investigations of multilayer MoS_2 transistors. We have seen here that the current saturation in our devices arises from a combination of usual electrostatics (i.e., pinch-off at the drain) supplemented by velocity saturation that becomes important as the channel mobility improves. Current saturation has also been reported for multilayer devices[5,7,18,20,34] and has similarly been discussed in terms of long-channel pinch-off[5] and velocity saturation.[34] However, the much higher mobility exhibited by multilayer MoS_2[37] results in saturated current values that may be >2 orders of magnitude larger[5,20,34] than those reported here. In this sense, it is clear that multilayer devices are more attractive than monolayer ones for applications requiring larger drive currents. Nonetheless, in spite of its lower mobility, monolayer MoS_2 benefits from a larger gap (1.8 eV) than its multilayer counterpart (1.2 eV), offering the potential of a lower off current. Additionally, and in contrast to multilayer MoS_2, its direct band structure makes monolayer material attractive for various light-emitting devices. In this sense, both monolayer and multilayer devices possess their own advantageous characteristics, making them suitable for very distinct applications.

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In conclusion, we have fabricated transistors from CVD-grown monolayer MoS_2 crystals and have demonstrated well-behaved operation in these devices. Excellent current saturation is observed at large drain voltages, and an analysis of the low-field transport indicates that the associated mobility is likely limited by scattering from charged impurities. The dominant conduction mechanisms are strongly dependent upon both the drain and gate biases with clear evidence of VRH at small V_d. With increases in both V_g and V_d, however, a satisfactory description of the characteristics can only be achieved by invoking the role of high-field velocity saturation. The velocity saturation was shown to arise from the presence of a strongly peaked electric field near the drain end of the channel, and the value of v_{sat} inferred from our studies was shown to be consistent with reports for multilayer MoS_2 transistors. This work therefore confirms the excellent potential of MoS_2 as a possible channel-replacement material and highlights the role of multiple transport phenomena in governing its transistor action.

■ ASSOCIATED CONTENT

Supporting Information

Information on the various devices studied, along with details of the simulation parameters, and a description of the mobility determination from the transfer characteristics. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b01159.

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Author Contributions

G.H. fabricated the MoS_2 transistors, and G.H., M.M., A.H., and N.A. measured their temperature-dependent electrical characteristics. G.H., R.S., H.R., G.B., S.N., R.V., and J.P.B. collaborated on the design of the experiments. K.G. performed the computational modeling of transistor performance, working in collaboration with U.S., G.H., and J.P.B. CVD growth of MoS_2 crystals was performed by S.N. in collaboration with R.V. and P.M.A. Y.G. and X.Z. performed AFM and Raman microscopy of the fabricated devices.

Notes

The authors declare no competing financial interest.

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