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Sub-100 nm integrated ferroelectric tunnel junction devices using hydrogen silsesquioxane planarization

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Ferroelectric tunnel junction (FTJ) is an emerging low power and nonvolatile memory device for beyond-complementary metal–oxide–semiconductor (CMOS) applications. The scalability of the FTJ devices need to be investigated for successful integration with CMOS for future nonvolatile circuits. In this article, a novel fabrication methodology is demonstrated to fabricate sub-100 nm FTJs. The fabrication process employs planarization with hydrogen silsesquioxane, an electron beam sensitive resist that is transformed into insulating material after curing. The method uses low temperature processes to minimize degradation of the device structures. The process is implemented to fabricate a Ti/$SrTiO_3$/$BaTiO_3$/$SrRuO_3$ FTJs of size $75 \times 75\,nm^2$, and the fabricated device shows ferroelectric switching with large ON/OFF ratio (∼125). © *2017 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4978519]

I. INTRODUCTION

As the dimensional scaling of Si CMOS devices reaches its limits, both emerging logic and memory devices are investigated for novel computing architecture for energy efficient computing.[1] In addition to scaling challenges of logic devices, Si CMOS based memory devices such as dynamic random access memory, NAND/NOR flash are also facing scaling challenges.[1–4] The International Technology Roadmap for Semiconductors has identified a number of low power and nonvolatile emerging memory devices that could potentially overcome the scaling limits of Si CMOS based memories.[1,3,5] Ferroelectric tunnel junction (FTJ) is one such noncharge based nonvolatile memory device that has the scaling potential for future beyond-CMOS circuits. The FTJ device uses the ferroelectric property to achieve nonvolatility.[6] However, unlike the destructive charge sensing of the capacitor in a FeRAM, it uses tunnel current measurement for nondestructive readout[7,8] of memory states. This has the potential for lateral scaling to sub-10 nm dimensions,[1] provided that ferroelectricity remains intact at these nanoscale dimensions.[9] Hence, the minimum lateral scaling of FTJs needs to be investigated in order to benchmark this device with other emerging memory devices.[1,2]

FTJ is a metal-insulator-metal (M_1-I-M_2) tunnel junction where the insulator material (I) is a ferroelectric oxide, and the polarization state of the ferroelectric barrier leads to different tunnel current densities and hence the two memory states.[6,10] The FTJ memory device figures of merit, which are the ON/OFF ratio, ON resistance, retention, and switching endurance, depend on the choice of the top and bottom metals,[10] the thickness of the ferroelectric oxide barrier,[11,12] and its magnitude of spontaneous polarization.[13] FTJs with $BaTiO_3$ (BTO) and $BiFeO_3$ ferroelectric barriers have been recently reported with large ON/OFF ratio and good retention characteristics.[11–14] However, there have been few reports on the scalability of the FTJs to nanoscale dimensions in a fully integrated device. Recently, an integrated BTO based FTJs with $300 \times 300\,nm^2$ size has been reported.[15] However, these devices need to be scaled down further for benchmarking with other memory devices.

Fabrication of two-terminal nanoscale FTJs requires different fabrication approaches compared to other existing two terminal resistive memory devices such as phase change memory (PCM).[16,17] In the case of PCM device fabrication, an additive process is used where the functional layer (phase change material) is directly deposited by sputtering during processing.[18] No corrosive etching or critical alignments is required to uncover top or bottom metals in this process. However, for integration of the FTJ device, a subtractive approach is necessary where the functional layer (ferroelectric oxide) and top metal (M_1) need to be etched to uncover bottom metal (M_2) during integration process.[15] This approach is necessary to maintain the epitaxial growth and crystal quality of the ferroelectric barrier. The ultrathin ferroelectric oxide layer, which is embedded inside M_1-I-M_2 structure, makes the integration challenging, and it requires reactive ion etching of the layers and stopping on the bottom metal (M_2) layer with minimal ion damage. Ion damage of the bottom metal is shown to affect the conductivity of the layer[19] and hence the device performance.[20] Moreover, as

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FTJ comprises perovskite oxide materials such as $SrRuO_3$ (SRO), $La_{0.67}Sr_{0.33}MnO_3$, and BTO, it must be processed at low temperature to avoid device degradation during metal contact formation.[19] Recently, fully integrated $\sim 300 \times 300\,nm^2$ FTJ memory based on Co/BTO/SRO heterostructure has been reported;[15] however, fabrication of sub-100 nm FTJ memory using the same process faces serious difficulties due to the sub-50 nm critical alignment between the contact pad to the nanoscale top contact. A new low temperature fabrication method is required to integrate sub-100 nm FTJ that eliminates steps of critical alignments, and this could be achieved with the planarization of the wafer with insulating low-k dielectric layers. In this article, we demonstrate a simple fabrication method to integrate sub-100 nm Ti/STO/BTO/SRO composite barrier FTJ using planarization with hydrogen silsesquioxane (HSQ)[21] electron beam resist. The fabrication method can be easily implemented to scale down FTJs laterally to sub-50 nm dimensions, and the method can also be used for fabrication of other emerging memory devices such as magnetic tunnel junction,[2,22] which require a subtractive approach for the functional layer.

II. FABRICATION

Prior to fabrication of FTJs, the STO (2 uc $\sim$ 0.77 nm)/BTO (6 uc $\sim$ 2.4 nm)/SRO (40 nm) heterostructure was grown epitaxially using a pulsed laser deposition (PLD) system on an atomically smooth TiO_2-terminated (001) STO substrate. To obtain atomically flat and TiO_2-terminated STO surface, (001) STO substrates were etched by buffered-HF for 1 min and were annealed at 900 °C for 6 h. The BTO and SRO thin films were grown on the annealed substrates by PLD. The epitaxial growth of all films here was monitored by *in situ* high pressure reflection high-energy electron diffraction intensity oscillations and patterns. During the BTO and SRO growths, the oxygen partial pressure in the PLD chamber was kept at 0.1 mbar. Subsequently, an ultra-thin STO layer of 2 uc was grown directly on top of the BTO thin film. A slightly lower oxygen partial pressure of 0.01 mbar was kept during the STO growth. After the growths, the samples were slowly cooled down to room temperature in an oxygen environment to minimize the formation of oxygen vacancy. Further details of the substrate preparation and growth process can be found in the previous reports.[15,23,24]

The sub-100 nm FTJ fabrication process flow is shown in Fig. 1. The process begins with a blanket STO ($\sim$0.77 nm)/BTO ($\sim$2.4 nm)/SRO (40 nm)/STO(001) FTJ heterostructure whose cross-section schematic is shown in Fig. 1(a). Sub-100 nm Ni/Au/Ti top contacts were defined using a JEOL 6300-FS (100 kV) electron beam lithography (EBL) system and subsequent electron beam metal depositions [Fig. 1(b)]. Ti is the top metal (M_1) for the intrinsic M_1-I-M_2 FTJ structure, while the Au ($\sim$120 nm) and Ni ($\sim$50 nm) are used to define the height of the structure necessary for planarization. Next, using Ni as the self-aligned etch mask, an inductively coupled plasma (ICP) reactive ion etching (RIE) system with BCl_3/Ar chemistry was used to remove the STO/BTO layers and stop on the conducting bottom metal (M_2) SRO. This process creates a nanopillar as shown in Fig. 1(c), with lateral dimension, $d < 100$ nm and height $h_p \sim 200$ nm. Next, the bottom Au contact pads are defined by EBL on the conducting SRO layer, which completes the intrinsic device definition [Fig. 1(d)]. In order to contact the top of the nanoscale device, a planarization with low-k dielectric such as HSQ (Ref. 25) is used here. The HSQ planarization process is shown in Figs. 1(e)–1(h). A 15% HSQ dissolved in methyl isobutyl ketone solution was chosen for planarization as it can provide thick HSQ layer with excellent planarity on a small sample ($5 \times 5\,mm^2$) which contains the nanopillar structures. The HSQ was spin-coated and baked at 150 °C temperature on a hotplate. The spin speed and time is chosen such that it coats $\sim$350 nm thick HSQ layer on a $\sim$200 nm nanopillar [see Fig. 1(e)]. Thicker HSQ layer gives better planarity (small step height, b_p) on a nonplanar structure; however, too thick HSQ layer (>800 nm) can cause excessive stress on the nonplanar surface, which may result in undesirable microcracks in the

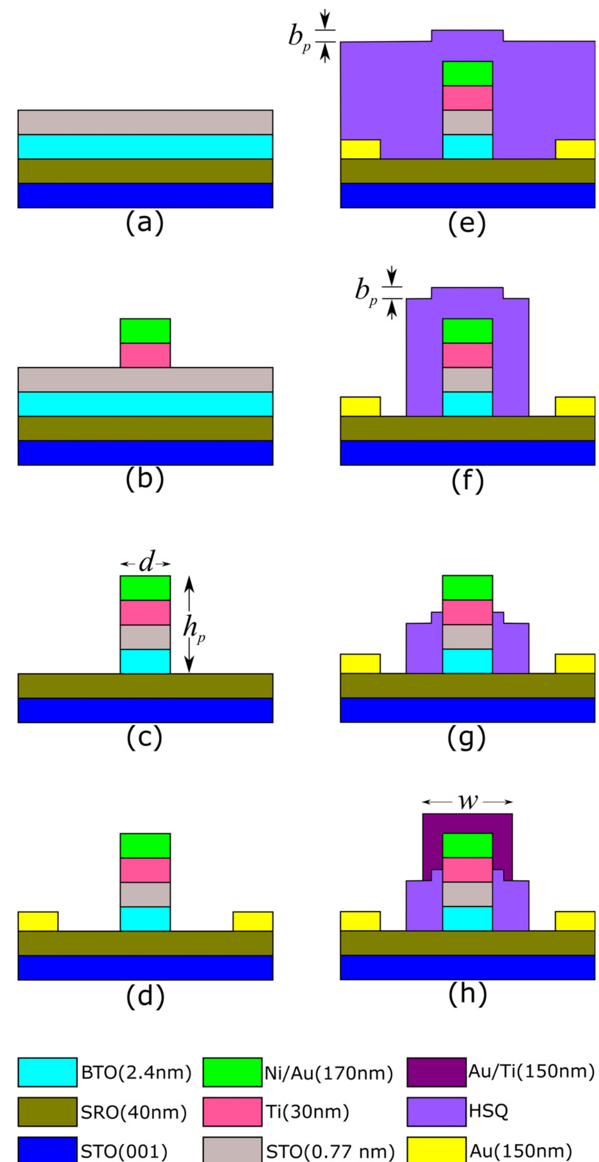

FIG. 1. (Color online) Schematic of sub-100 nm FTJ fabrication process flow [(a)–(h)].

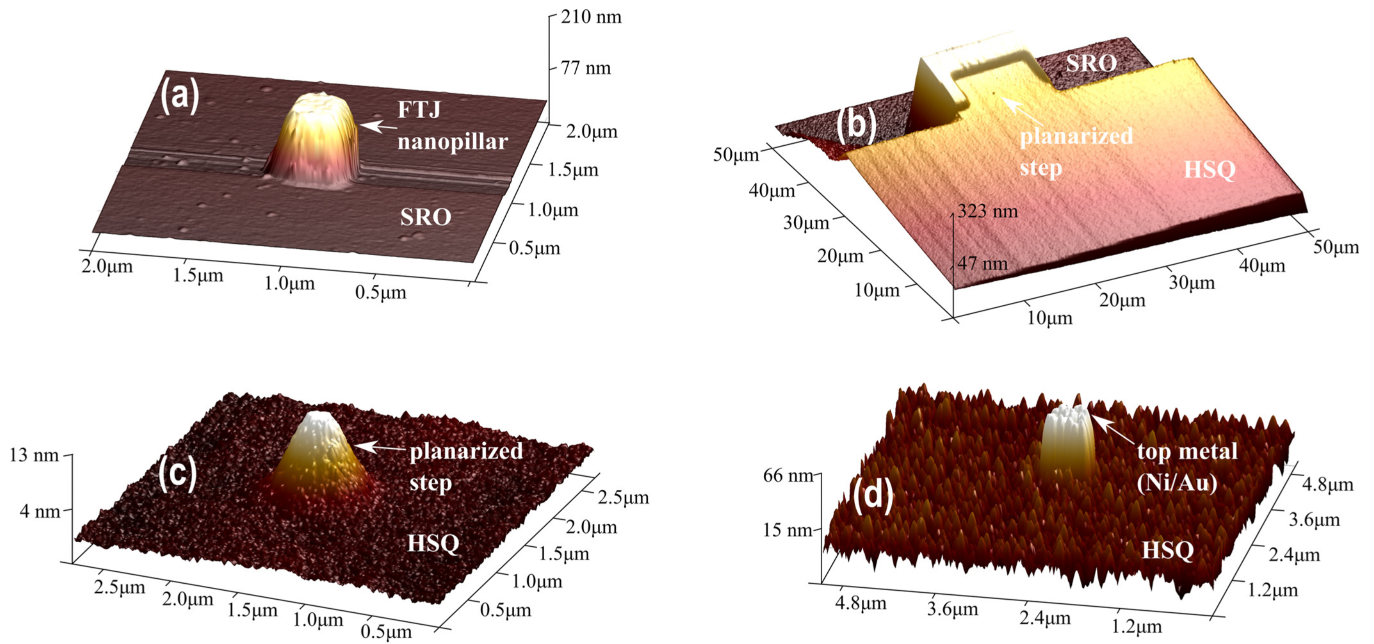

FIG. 2. (Color online) AFM images of (a) FTJ nanopillar of height ~200 nm before planarization, (b) planarized step after planarization by HSQ and EBL exposure, (c) close-up-view of the planarized nanopillar, step height is measured to be ~10 nm after planarization, and (d) after etch back of HSQ to open up top 50 nm (Ni/Au) of the nanopillar.

HSQ.[26] After spin coating and soft baking, EBL was used to expose HSQ on the selected region so that it converts to an insulating films.[27] After development in tetramethylammonium hydroxide solution, a planarized insulating film is left on top of the nanopillars as shown in Fig. 1(f), with a small nonplanar step height, b_p of ~10 nm. This process leads to a planarity ratio[28] $(1 - b_p/h_p)$ of 95% which is excellent without using any chemical mechanical planarization for small $(5 \times 5\,\text{mm}^2)$ sample. A low temperature (200 °C) thermal curing was carried out next to densify the films. In contrast, the phosphosilicate glass based planarization process needs higher temperature reflow to achieve insulating properties.[25,29] Next, a blanket RIE was performed using CF_4 and O_2 gas mixture of 20 and 5 sccm, respectively, to etch back HSQ to uncover the top metal of the nanopillars. The ICP and RIE power was chosen 25 and 50 W, respectively, which ensures minimum ion damage to HSQ surface. The etching time was chosen such that only ~200 nm HSQ was etched from the top, which exposes a ~50 nm of FTJ nanopillar [Fig. 1(g)]. The bottom contact pad is defined on the SRO layer [Fig. 1(d)], while the top contact pad is defined on the remaining ~150 nm thick HSQ. An EBL and lift-off was performed to define Au/Ti (~150 nm) top contact pads on the insulating HSQ to contact the FTJ nanopillar [Fig. 1(h)]. As the top contact pad is on an insulating layer, the alignment tolerance for this process is in the micron scale ($w \sim 5\,\mu m$) eliminating sub-50 nm precision alignment steps required in the previous process flow.[15]

Planarization process described in Figs. 1(e)–1(h) was verified step by step using an atomic force microscope (AFM) shown in Fig. 2. The height of the nanopillar after performing self-aligned etch is measured to be ~200 nm [Fig. 2(a)]. After planarization of the nanopillar, the top surface of HSQ is flat as seen in Fig. 2(b) with a small step height ~10 nm, [see Fig. 2(c)]. Finally, after CF_4/O_2 RIE etch back of the HSQ, ~50 nm of the nonpillar is exposed as seen in Fig. 2(d). The scanning electron micrograph (SEM) images show different steps of FTJs fabrication with HSQ planarization (Fig. 3). A $75 \times 75\,\text{nm}^2$ Ti/Au/Ni FTJ nanopillar is shown in Fig. 3(a) after the self-aligned etch. The top view SEM image of a $500 \times 500\,\text{nm}^2$ FTJ after HSQ

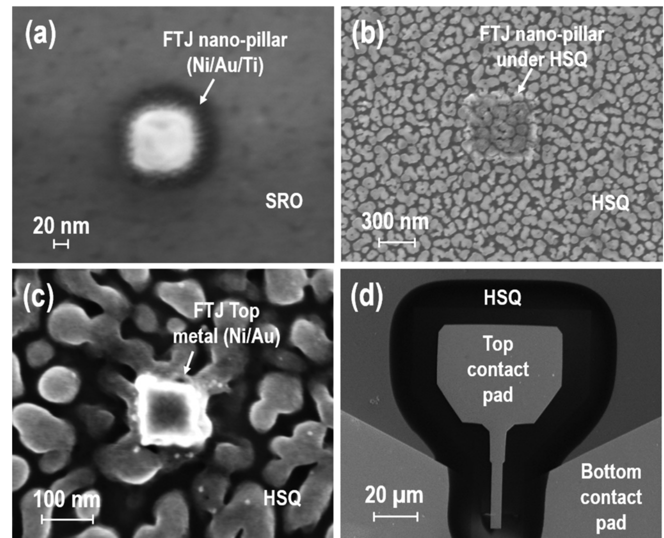

FIG. 3. SEM image of (a) FTJ nanopillar of size $75 \times 75\,\text{nm}^2$ before planarization, (b) top view of a $500 \times 500\,\text{nm}^2$ FTJ nanopillar submerged under HSQ with grain size $\sim 100 \times 100\,\text{nm}^2$ after planarization and EBL exposure, (c) opening of a sub-100 nm FTJ nanopillar's top metal (Ni/Au) after HSQ etching, and (d) a fully integrated Ti/STO/BTO/SRO FTJ device with contact pads for measurement.

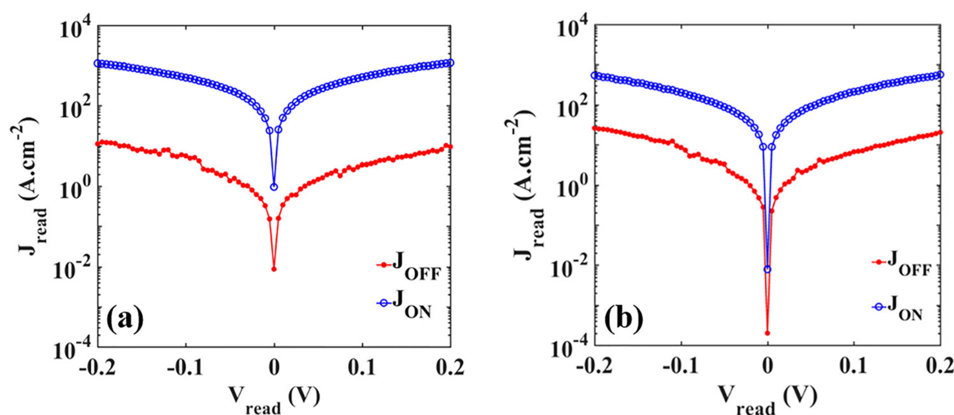

FIG. 4. (Color online) Measured J-V characteristics of (a) $75 \times 75\,nm^2$ and (b) $150 \times 150\,nm^2$ FTJ in ON and OFF memory states, showing large ON/OFF ratios. The write voltage amplitudes were ± 5 V with 100 ms poling pulses.

planarization is shown in Fig. 3(b). The opening of top metal Ni/Au (∼50 nm) of a sub-100 nm FTJ after CF_4/O_2 RIE is shown in Fig. 3(c). A fully integrated FTJ with top and bottom contact pads are shown in Fig. 3(d). The exposed and cured HSQ layer provides the required electrical isolation between the top and bottom contact pads. Both sub-100 nm and $500 \times 500\,nm^2$ devices were fabricated showing the repeatability of the process.

III. MEASURMENT AND RESULTS

To verify the new process, a full scale FTJ fabrication process was carried out on a Ti/STO/BTO/SRO heterostructure discussed previously and its electrical characteristics were measured. The current voltage (I-V) measurement was performed on a $\sim 75 \times 75$ and $\sim 150 \times 150\,nm^2$ FTJ using HP4155B semiconductor parameter analyzer on a JR2745 microwave probe station. The insulating properties of the EBL exposed HSQ was first confirmed by measuring the leakage current through ∼350 nm HSQ, the leakage current density was $\sim 4\,\mu A/cm^2$ at ± 5 V, which is orders of magnitude smaller than the write/read current density of FTJs. The ON/OFF memory states of FTJ were measured at the read voltage of 0.2 V, while the write voltages were 100 ms pulses of ± 5 V. The measured current–voltage characteristics is shown in Fig. 4, the ON current densities for a 75×75 and $\sim 150 \times 150\,nm^2$ Ti/STO/BTO/SRO FTJs during the read operation were measured as $J_{ON} \sim 10^3\,A/cm^2$ and $J_{ON} \sim 0.5 \times 10^3\,A/cm^2$, respectively, which is consistent with a constant resistance area product ($RA \sim 10^{-4}\,\Omega\,cm^2$). The nonvolatile memory state of FTJ was changed from ON to OFF by applying a write voltage of +5 V with 100 ms pulse width. The OFF current densities for a 75×75 and $\sim 150 \times 150\,nm^2$ were measured to be $J_{OFF} \sim 8\,A/cm^2$ and $J_{OFF} \sim 20\,A/cm^2$, respectively. Both the ON and OFF current densities of measured devices are many orders of magnitude larger than the leakage current density through EBL exposed HSQ. The maximum ON/OFF ratio was measured ∼125 for a $75 \times 75\,nm^2$ FTJ. The measured electrical characteristics of the FTJ show the suitability of the HSQ planarization process as the back end of the line technology for FTJs.

IV. CONCLUSIONS

A sub-100 nm fabrication process is described using planarization of HSQ to integrate Ti/STO/BTO/SRO composite barrier FTJ of size $75 \times 75\,nm^2$. The process is verified by switching measurements of FTJ device with large ON current density ($J_{ON} \sim 10^3\,A/cm^2$) and small OFF current density ($J_{OFF} \sim 8\,A/cm^2$). The process avoids critical sub-50 nm alignment. The low temperature process reduces any device degradation during metal contact formation. The developed fabrication method is also useful to integrate two terminals beyond CMOS devices with emerging materials which require a subtractive process for functional material.

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