IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Received 3 November 2017; revised 15 December 2017, 23 January 2018, and 14 February 2018; accepted 21 February 2018.
Date of publication 27 February 2018; date of current version 26 March 2018.

Digital Object Identifier 10.1109/JXCDC.2018.2809640

Towards a Strong Spin–Orbit Coupling Magnetoelectric Transistor

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This work was supported in part by the National Science Foundation through NSF-ECCS under Grant 1740136 and Grant 1508541, in part by the Nebraska Materials Research Science and Engineering Center under Grant DMR-1420645, and in part by the Nanoelectronics Research Corporation, a wholly owned subsidiary of the Semiconductor Research Corporation, through the Center for Nanoferroic Devices, an SRC-NRI Nanoelectronics Research Initiative Center. The work of X. Hong was supported by the U.S. Department of Energy, Office of Science, Basic Energy Sciences, under Award DE-SC0016153. The work of K. L. Wang and C. Binek was supported by ARO through MURI under Grant W911NF-16-1-0472. This paper has supplementary downloadable material available at http://ieeexplore.ieee.org., provided by the author. This includes additional remarks to the paper and additional schemes of devices. This material is 315 KB in size.

ABSTRACT Here, we outline magnetoelectric (ME) device concepts based on the voltage control of the interface magnetism of an ME antiferromagnet gate dielectric formed on a very thin semiconductor channel with large spin–orbit coupling (SOC). The emphasis of the ME spin field-effect transistors (ME spin FET) is on an antiferromagnet spin–orbit read logic device and a ME spin-FET multiplexer. Both spin-FET schemes exploit the strong SOC in the semiconducting channel materials but remain dependent on the voltage-induced switching of an ME, so that the switching time is limited only by the switching dynamics of the ME. The induced exchange field spin polarizes the channel material, breaks time-reversal symmetry, and results in the preferential charge transport direction, due to the spin–orbit-driven spin-momentum locking. These devices could provide reliable room temperature operation with large on/off ratios, well beyond what can be achieved using magnetic tunnel junctions. All of the proposed device spintronic functionalities without the need to switch a ferromagnet, yielding a faster writing speed (∼10 ps) at a lower cost in energy (∼10 aJ), excellent temperature stability (operational up to 400 K or above), and requiring far fewer device elements (transistor equivalents) than CMOS.

INDEX TERMS Magnetoelectric (ME) transistor, nonvolatile logic and memory, spin–orbit coupling (SOC).

I. INTRODUCTION

MODERN dynamic random access memory elements are volatile and require frequent refresh power. On the other hand, a solid-state device with a magnetically ordered state could be engineered into a memory or logic element whose information is nonvolatile. For example, magnetic random access memories (MRAMs) are advanced in terms of access time and endurance and do not require continued power to store information. MRAMs have significant deficiencies, however, in terms of power consumption due to their high writing energy. Although major advances have been achieved in recent years by progressing from switching via Oersted fields to spin transfer or spin–orbit torques, these devices still require large current densities [1]–[5]. Current densities in excess of 1 MA/m^2 are required for writing of the magnetic state in spin-transfer-torque memory elements [6] and, consequently, are not energy efficient. Conventional schemes of nonvolatile magnetic memories and logic largely rely on the functionality of magnetic tunnel junctions (MTJs)—key devices of modern spintronic technologies. MTJ operation is based on the switching of a free ferromagnetic (FM) layer, resulting in a change of its tunnel-

ing resistance. The speed of this operation is determined by the time required to rotate the magnetization of the nanomagnet, which is typically a few nanoseconds. This is nearly 3 orders in magnitude slower than the time required to charge a capacitor, as implemented in complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs).

Based on the discussion above, it would be desirable, on the one hand, to provide nonvolatility of the state variable of the device, and on the other hand, be able to switch this state with low power and high speed. By adopting a transistor geometry, based solely on the switching of a magnetoelectric (ME), switching speed can be limited only by the switching dynamics of that material, thereby avoiding the long delay times plaguing other spintronic devices that rely on the slower switching delay (as long as 5 ns) of a FM layer. Moreover, the devices discussed here promise to provide a unique FET-based interface for input–output of other novel computational devices that depend on magnetics (e.g., magnetic cellular logic [7]). This is spintronics without a ferromagnet, with faster write speeds (<20 ps/1 bit of a full adder), at a lower cost in energy (<200 aJ/1 bit of a full adder), greater temperature stability (operational to 400 K or more), and scalability, requiring far fewer device elements (transistor equivalents) than CMOS.

ME materials also provide a unique way to read out and transmit information through roughness-insensitive boundary magnetization, which is intrinsically coupled to the anti-FM order. As has been demonstrated in [8] and [10]–[15], electrical switching of the AFM order parameter is accompanied by reversal of boundary magnetization, which allows for a plethora of functionalities and novel device concepts.

More conventional ME spin transistors have been proposed previously [16]–[19], but those studies have not emphasized the value of using a narrow channel conductor with strong spin–orbit coupling (SOC) to enhance the on/off ratio. Manipatruni *et al.* [20] proposed a device based on the combination of an ME dielectric layer and an SOC channel. However, that scheme does not involve direct coupling between the ME and SOC materials. The latter is used as a transduction mechanism from the state of a ferromagnet to an electric signal. Another proposed device scheme involves the detection of the interface spin current due to the anomalous Hall effect in a paramagnetic layer on top of the ME chromia [11], [12], which also did not explicitly exploit the spin-Hall effect of a conduction channel with large SOC.

There are several theoretical proposals to utilize voltage-controlled exchange bias in heterostructures, which use an ME antiferromagnet and an exchange coupled FM layer as the fundamental building block of memory and logic devices [1], [21]–[36]. Exchange coupling between the boundary magnetization of the antiferromagnet and the FM layer allows for the voltage control of the latter's magnetization, which then serves as a nonvolatile state variable. This writing mechanism avoids dissipative currents and is thus energy efficient and inerts against detrimental effects from Joule heating. Symmetry constraints rigorously imply

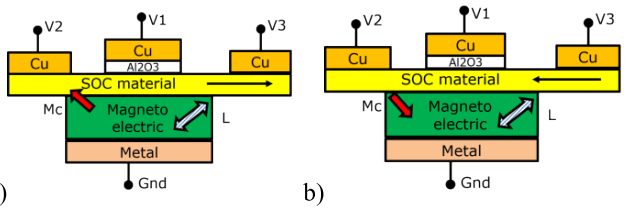

FIGURE 1. Scheme of AFSOR logic. (a) State with positive V_1 applied and the surface or interface magnetization of the ME gate M_{surf} pointing up. (b) State with negative V_1 applied and surface magnetization M_{surf} pointing down.

that the reversal of magnetization, which is odd under time inversion, cannot be achieved by a quasi-static electric field, which is even under time inversion. Pathways to overcome this fundamental problem include successive 90° magnetization rotation, timed voltage pulses exploiting voltage-controlled anisotropy, and magnetization precession. In contrast, we employ small static applied magnetic field breaking time inversion when utilizing voltage-controlled switching of boundary magnetization in ME antiferromagnets. The symmetry breaking magnetic field can be as low as earth's magnetic field. The dipole field of a fixed ferromagnet can be utilized as a robust field source. For instance, the bottom metallic layer of the AFSOR shown in Fig. 1 can be designed to be FM but exchange decoupled thus serving as an electrode and magnetic field source.

The most commonly discussed readout mechanism relies on tunneling magnetoresistance (TMR), where the voltage-controlled FM film constitutes the free layer of the TMR trilayer [1], [22]–[26], [31]–[37]. Problems arise with leakage currents, canted magnetization (as may occur with very high critical temperature MEs), and when scaling to very small dimensions. In the latter case, the AFM volume decreases. As a result, maintaining the required reversible ME energy for switching requires an increase of the electric field. However, dielectric breakdown prevents application of electric fields above a few MV/cm.

II. ANTIFERROMAGNET SPIN–ORBIT READ (AFSOR) LOGIC DEVICE

Switching of any induced spin polarization is a key element of the proposed ME spin-FET architectures that we discuss here. The idea is to exploit voltage control of spin polarization that has been induced via interface exchange in a thin semiconducting channel. The ME material can be ferroelectric (e.g., $BiFeO_3$) or a dielectric (e.g., Cr_2O_3). Switching of the induced spin polarization is virtually instantaneous, which is the major advantage over the much slower precessional switching of remnant magnetization (typically a few nanoseconds, but no faster than 178 ps [29] to 500 ps [38]). Switching speed is, therefore, only limited by the reversal of the AFM order parameter. The higher AFM resonance frequency indicates that switching of antiferromagnets is intrinsically much faster than switching of ferromagnets. The onset of the source–drain current with voltage, i.e., transistor operation,

will be extremely sharp, because the ME switching has a very sharp nonlinear response to applied voltage [9], [39]. The antiferromagnet spin–orbit read (AFSOR) logic device structure (Fig. 1) has the following intriguing features: the potential for high and sharp voltage "turn on"; inherent nonvolatility of magnetic state variables; absence of switching currents, which lowers power consumption; large on/off ratios; and multistate logic and memory applications. The design will provide reliable room temperature operation with large on/off ratios well beyond what can be achieved using MTJs. The core idea here is to use the boundary polarization of the ME to spin polarize or partly spin polarize a narrower (very thin) semiconductor.

Requirements for the material are as follows:

1) large SOC;
2) topological protection of conducting states;
3) spin polarization control by voltage;
4) scalability, i.e., reasonable conduction even in narrow wires <10 nm.

The roughness-insensitive boundary magnetization at the interface between the ME film and the narrow channel semiconductor or paramagnetic overlayer is strongly coupled to the bulk AFM order parameter and follows the latter during voltage-controlled switching [8], [11], [12]. If the narrow channel conductor is sufficiently thin, the transport channel will be spin polarized by a proximity effect [16], [24], [40], [41]. Quantum–mechanical exchange coupling between the boundary magnetization and the carrier spins in the narrow channel of the FET can give rise to a damped precession of the spins injected from the source of the FET. When utilizing channel materials with weak SOC, such as graphene or Si, the effective exchange field of the voltage-controlled boundary magnetization is the sole source for spin precession. If the semiconductor channel retains large SOC, then the spin current, mediated by the gate boundary polarization, may be enhanced and, to some extent, topologically protected. The latter implies that each spin current has a preferred direction. Modulated spin precession, and added functionality is possible if SOC is exploited, such as in BiSeTe and the transition metal dichalcogenides (TMDs), as would be the case in the ME multiplexer that is discussed later.

Both the *AFSOR logic* device and the *ME spin-FET multiplexer (spin-MUX)* exploit the modulation of the spin–orbit splitting of the electronic bands of the semiconductor channel materials through a "proximity" magnetic field derived from a voltage-controlled ME material. We utilize the electrically switchable and nonvolatile boundary magnetization of an ME antiferromagnet, such as chromia [8], to generate a voltage-controlled exchange field, which determines the carrier spin in the conducting channel (Fig. 2). For a given remanent boundary magnetization, the exchange field will determine the spin state of the carriers at the analyzer (drain) in concert with the length of the channel (Fig. 1), while SOC could be exploited to determine the direction of current flow (Fig. 3). The combination provides a class of nonvolatile

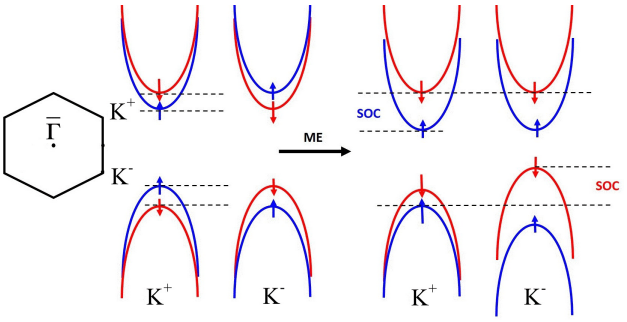

FIGURE 2. Schematic of exchange splitting induced by the boundary magnetization of an ME such as chromia, in a 2-D channel system with large SOC. The induced polarization is altered at $K+$ and $K-$ points of the Brillouin zone by a Zeeman-like effect, so the channel, in a material like WSe_2, is nearly 100% polarized at the top of the valence band.

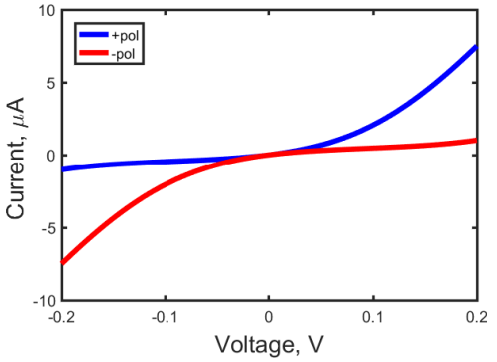

FIGURE 3. Source to drain current versus voltage V_1 in the AFSOR device of Fig. 1. The SOC channel polarized in opposite directions (+ or –) by the ME gate.

digital circuits that resemble multiple collector bipolar junction transistors [42] or might be considered as nonvolatile, low-power merged transistor logic, but with the advantage of being a planar technology. With variants of the device of Fig. 3, where inversion symmetry is not so strictly broken, one can imagine a modern version of multiplexer logic (MUX), with the added bonus of nonvolatility.

The operational procedure of the AFSOR logic device is outlined as follows. To write the state, a positive or negative voltage V_1 is applied to the cell of Fig. 1. In response to the electric field associated with this voltage, paraelectric polarization as well as the AFM order (L) in the ME insulator (such as chromia, Cr_2O_3) are switched. Surface magnetization (M_{surf}), tied to the value of L, polarizes the spins of carriers in the SOC material and induces preferred conduction, i.e., much lower resistance, in only one direction along the SOC channel. In other words, the influence of M_{surf} on the channel produces directionality of conduction, which is not possible through conventional gate dielectrics, as indicated in Fig. 3. The current versus voltage dependent on the direction of ME polarization is obtained by NEGF transport simulation [27] in a 2-D ribbon with a width of 20 nm and a

band mass of $0.1m_e$, for illustration we assume a conservative value of exchange splitting of 0.1 eV, $V_3 - V_2 = 0.1$ V, at 300 K. To read the state, a positive or negative voltage $V_2 - V_3$ is applied between the source and drain of the devices. The charge current mainly flows in the low-resistance direction. The current conducted in the channel is used to charge the next stage of capacitors, and in turn switch the AFM in these elements. Thus, the AFSOR elements are easily cascaded. The use of a 2-D material as the channel gives much better control of conductivity by boundary polarization M_{surf}. Unidirectional conductance has been demonstrated in a ferromagnet/topological insulator heterostructure [43]; and a similar effect in ferromagnet/spin-Hall metal heterostructure [44]. As noted above, to break symmetry, the dipole field of a fixed ferromagnet can be utilized. For the AFSOR, shown in Fig. 1, the bottom metallic layer of the gate can be designed to be FM, but exchange decoupled thus serving as electrode and magnetic field source. Quantum–mechanical exchange and the corresponding exchange field depend on orbital overlap giving rise to an exponentially fast decay with separation of the exchange coupled atoms. The magnetic dipole field, in contrast, decays algebraically and is long range in comparison with the exchange field. It is, therefore, straightforward to achieve decoupling between a FM electrode and an adjacent antiferromagnet. An interlayer of just one unit cell of Al_2O_3 can effectively disrupt exchange interaction between the ferromagnet and the antiferromagnet and at the same time serve as lattice matching seed layer for the epitaxial growth of chromia.

This device exploits the spin of the electron (or hole) by utilizing the nonvolatile switching of ME gates to influence the exchange splitting in a large atomic number Z and a narrow channel conductor with SOC. Those include materials such as WSe_2, HfS_3, $(Bi_{1-x}Sb_x)_2Te_3$, In_4Se_3, In_4Te_3, or the electron gas that forms at the surface/interface of InP and InAs, ideally systems where there is strong SOC. Nonvolatility in such possible devices comes from the ME gate, while the ME sensing effect comes from the voltage control of the large SOC. Spin-Hall effect as a means of translating SOC into spintronic devices has been discussed for decades [45]–[47], but only realized fairly recently [48]–[50] for 3-D materials and heterointerfaces, not narrow channel 2-D materials where the effect might be expected to be much larger.

Compared to prior spin-logic devices, the advantages of AFOSR are that the AFM order is not sensitive to external magnetic fields and its switching is not affected by sidewall roughness. By avoiding a ferromagnet channel and FM switching, the write operation is much faster, ~3–20 ps [29], [51]. Switching of the induced spin polarization, therefore, has the major advantage to be virtually instantaneous when compared with the precessional switching of remnant magnetization (typically nanosecond but no faster than 178 ps [29] to 500 ps [38]),

In the proposed device scheme, even a single gated device would enable high on/off ratios, as described [52], [53]. Since the spin current undergoes a lateral force, spin up and down are separated and could be "read" by "split drains," although the use of spin-polarized drain electrodes will clearly enhance the on/off ratio of the drain current and the spin-Hall voltage (voltage at one drain minus the voltage at the other drain). This spin-Hall voltage will be very material dependent. In a material like WSe_2, the spins would be defined perpendicular to the plane, so that the magnetized drain electrode should, in the simplest implementation, have magnetization perpendicular to the plane as well. This would align with the induced spin polarization from an ME like chromia, which is also perpendicular to the plane. Note that if a FM contact is used, there would be no "switching" of this contact, in normal device operation.

The AFSOR (Fig. 1) device uses a Zeeman-like perturbation of the SOC in the channel (schematically illustrated in Fig. 3, for a transition metal dichalcogenide) to modulate spin polarization in the device. The output is a voltage difference when SOC is "turned on" between the two FM drain contacts due to the spin-Hall effect. This output voltage can be modulated by the gate or gates (when top and bottom gated), which influences the spin–orbit interaction in the channel. Such control will be especially effective when involving both top and bottom gates. The spin-Hall voltage in the device can be increased by using different FMs in the source and drain. By adopting a scheme based solely on ME switching, its speed will be limited only by the switching dynamics of the ME (somewhere in the region of 10–100 ps [20]).

Magnetization in the conduction channel with SOC is switched by precessional switching [54]. The effective spin polarization in inverse Rashba–Edelstein effect is

$$P_{\text{eff}} \sim w \times \lambda/d \sim 60\ \text{nm} \times 0.5/3\ \text{nm} \sim 10 \qquad (1)$$

where w is the width of the magnet, d is the thickness of the spin–orbit channel, and $\lambda \sim 0.5$ is the spin–orbit coefficient for Bi_2Se_3. Then the charge required for switching is

$$Q_{\text{fm}} = eN_s/P_{\text{eff}} \sim 1.6 \times 10^{-19} \times 1 \times 10^4/10 \sim 160\ \text{aC} \qquad (2)$$

for a magnet with $N_s = 10^4$ spins (Bohr magnetons). Current delivered by a present day transistor at a drain voltage of 0.1 V can be as large as 6 μA. Then, the pulse needed to conduct this charge can be shorter than 20 ps, but depends critically on the leakage through the ME gate dielectric—the greater the resistance of the ME, the faster the switching speed and the smaller the energy cost.

Transistors typically have better on/off ratios than a tunnel junction device. As such, they have greater potential for use in logic devices, than a spintronic device based on a tunnel junction. on/off current ratio in 2-D FETs is experimentally shown to extend up to 10^8 for MoS_2 [55] and 10^6 for WSe_2 [56], while magnetoresistance effect in MTJs does not exceed 10^2. As the exchange splitting in the 2-D channel of the transistor approaches the value of the surface potential change in a FET, one expects similar on/off ratio.

The induced spin polarization of the channel can be altered by changing the boundary polarization of the gates, and

manipulated by using the ME properties of the gates. The SOC can be changed by the electric field across the channel, and the current channel can be turned off by the net bias applied to the channel. This multistate memory or logic is especially robust if the source is spin polarized as well, although the magnetization of the source is by no means essential for the overall device to work, as spin injection is *not* essential. The advantage of this device over conventional spin-FET devices is that the output voltage can be directly used to drive the next stage in a circuit, without the need for additional devices. This will help in reducing the device count in logic circuits. Another advantage of using channel materials with large SOC is that the SOC can lead to enhanced carrier mobility, as the spin flip scattering is then much suppressed at room temperature.

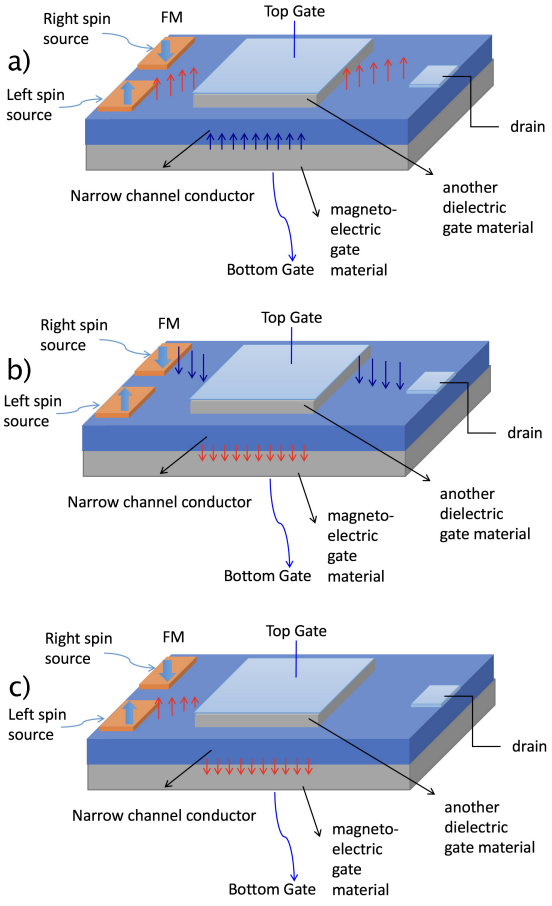

FIGURE 4. Basic nonvolatile ME spin MUX, with FM source contacts. The thin channel conductor/semiconductor (blue) would be polarized (a) up or (b) down. (c) Spin-polarized current in the opposite sense from the polarization induced by the ME gate is blocked. Device considerations favor semiconductors with large SOC, where the boundary polarization alters the SOC and polarizes the channel, as indicated in Fig. 5 [24], [51].

III. MAGNETOELECTRIC SPIN-FET MULTIPLEXER

In a variant of Fig. 1, where inversion symmetry is not as strictly broken as in the case of Fig. 4, one can imagine a modern version of MUX, with the added function of nonvolatility. The *ME spin MUX* (Fig. 4) also exploits the modulation of the spin–orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled ME material. Here, by using semiconductor channels with large SOC, we expect to obtain a transverse spin-Hall current, as well as a spin current overall. Depending on the magnitude of the effective magnetic field in the narrow channel, we anticipate two different operational regimes. Like the AFSOR ME spin FET, the ME spin MUX in Fig. 4 uses SOC in the channel to modulate spin polarization and hence the conductance (by spin) of the device. There is a source–drain voltage and current difference, between the two FM source contacts, due to the spin-Hall effect when SOC is present. This output voltage can be modulated by the gate or gates, which influences the spin–orbit interaction in the channel especially when it is both top and bottom gated especially. The spin-Hall voltage in the device can be increased by using different FMs in the source and drain.

In addition to being configured as a logic element, this device can also be used to provide multivalued logic as the source can be turned on or off either by different combinations of gate electrode voltages, or by switching of the boundary polarization of the ME gate. As a logical device, the ME spin MUX has two inputs—the direction of magnetization in the channel as a result of the boundary polarization and the voltage at the gate. Up and down directions of magnetization are designated as "0" and "1." Also the two directions of the polarization (switched by voltage, e.g., 0 and 0.1 V) producing opposite values of SOC in the channel are designated as "0" and "1." Note that these states are nonvolatile, i.e., the state condition remains even when the power is turned off. The advantage of this device over conventional spin-FET devices is that the output voltage can be directly used to drive the next stage in a circuit, without the need for additional devices. This will help in reducing the device count in logic circuits. A schematic view of the variations of these ME devices is shown in Fig. 4, which utilize the atomic-scale thickness of 2-D crystals for spintronic applications. The on/off ratio of spin FETs is known to be degraded by low spin injection efficiencies, as noted above, caused by the spin-conductivity mismatch between their FM contacts and the nonmagnetic (NM) semiconductor channel [57]. This mismatch might be circumvented by inserting a thin tunnel barrier between the FM contact and the semiconductor, allowing the barrier-related resistance to dominate.

Several other types of devices in which a ferroelectric gate controls a channel with spin orbital coupling are described in the supplementary material.

IV. INDUCED POLARIZATION

While 2-D materials are an attractive channel material choice, because of the reduced source to drain "crosstalk" or leakage current at very small spatial dimensions [58], [59], in the devices discussed here, they are extremely attractive because

they are atomically thin and the induced polarization in the channel is very high, as indicated in Fig. 2. This is essential to the device concepts just discussed, but does not represent the limits imposed by the key challenges that must be addressed.

Another challenge lies in maintaining the ME spin-FET device characteristics while scaling the device dimension to less than 10 nm. For this purpose, we favor HfS_3, In_4Se_3, In_4Te_3, or the electron gas that forms at the surface/interface of InP and InAs as SOC channel materials, because they are likely to be scalable to spatial channel widths of 10 nm or less. Concern about edge scattering has attracted the attention of theorists [60]–[65] and has been found to have a major influence in experiment [66]–[68]. The trichalcogenides, MX_3, and other transition metal trichalcogenides (TMTCs) such as In_4X_3 (X = Se, Te) possess a unique quasi-1-D structure that makes devices scaled to dimensions less than 10 nm appear possible.

There are several reasons to seriously consider materials from the transition metal TMTC family. These trichalogenide materials are also layered materials but the edge structure and edge chemistry lend the ribbon greater fidelity and fewer imperfections. While the topological insulators may be suitable channel materials for the AFSOR logic device of Fig. 1, as they do exhibit a topologically protected spin current, likely the better device performance will be achieved using TMTC's. The TMTC's not only possess a unique quasi-1-D structure, but also have promising semiconductor properties. For example, TiS_3 has a bandgap of $\sim$1 eV [69], while In_4Se_3 has a direct bandgap of about 1.3 eV [70], [71] and an indirect gap of about 0.6 eV [72]–[74], making the bandgaps of both TiS_3 and In_4Se_3 comparable to that of silicon (1.1 eV). Also, according to a recent theoretical study, in the direction along TiS_3 chains, titanium trisulfide is expected to have higher electron mobility of $\sim$10 000 cm^2/Vs [70]. HfS_3, with a crystal structure similar to TiS_3, will also possess highly anisotropic crystal structure and might be a suitable choice TMTC material for the development of the AFSOR logic device of Fig. 1, because of the expectation of large SOC (the Z of Hf is far larger than that of Ti). This is extremely promising because single-layer titanium trisulfide TiS_3 FETs have been fabricated [75]. These TMTC channel materials are viewed as advantageous as they combined significant SOC and a minimum or edge scattering. It should be noted that in the case of various topological insulators, edge scattering will actually increase the influence of SOC, and a thin layer TI will form a bandgap [76] thus, should the chemical potential fall mid gap, retain the desire high on/off ratios. Without the bandgap, the topological insulator material/channel will act more like a spin valve and suffer from a decrease in on/off ratio and spin fidelity, in the limit of small spatial dimensions, in spite of the very large SOC.

As noted above, key to the ME devices is the proximity induced polarization [16], [24], [40], [41], [76]–[78] in the narrow (2-D) conduction channel. Not all of the proposed 2-D semiconductor channel materials have been

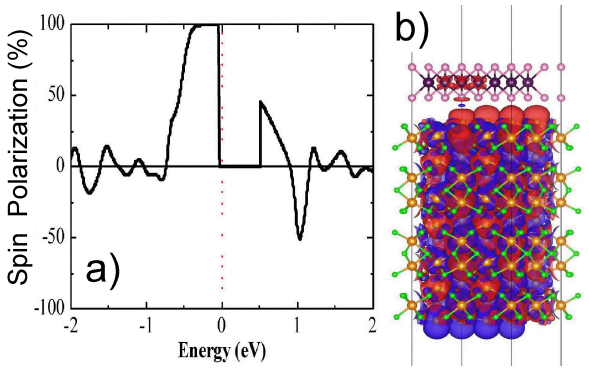

FIGURE 5. Induced spin polarization in WSe_2,by the boundary magnetization of chromia. The induced polarization is altered at $K+$ and $K-$ points of the Brillouin zone (Fig. 2), by a Zeeman-like effect, so the (a) WSe_2 channel is nearly 100% at the top of the valence band (for hole conduction) through (b) interaction with chromia.

modeled, but as proof of principle, induced polarization in MoS_2 and WSe_2, in contact with chromia has been modeled, as indicated in Fig. 5. We constructed a Cr_2O_3 (0001) slab model with 11 Cr layers and 10 O layers, in which the outmost layers are Cr ones, in accordance with the previous studies [16]. For the heterostructures of TMD monolayer on top of Cr_2O_3 (0001) slab, we adopted a 3×3 TMD supercell to match the 2×2 Cr_2O_3 (0001) slab supercell. The lattice mismatch for WSe_2/Cr_2O_3 was 0.3%, which was applied to the lattice constant a of Cr_2O_3 (0001) slab in order to match the TMD supercells, since the electronic properties of TMDs are very sensitive to the lattice constant a, whereas the bandgap changes of Cr_2O_3 (0001) slab on lattice constant a are negligible.

All calculations were performed within the framework of the Vienna *ab initio* simulation package VASP [79]–[81], a first-principle plane-wave code based on spin-polarized density functional theory (DFT). The exchange correlation was treated with the Perdew–Burke–Ernzerhof functional [81], and the projector augmented wave method was used to describe the interaction of electron ion. A plane-wave basis set with the energy cutoff of 400 eV was adopted in the calculations. The vdW corrections [82], [83] and dipole corrections [84], [85] were performed for both heterostructures. To correct the strong on-site electronic correlation, the DFT + U method was used for the Cr atoms with $U - J = 4$ eV. The Brillouin zone integration is performed using Monkhorst–Pack [86] $4 \times 4 \times 1$ grid for geometry optimizations and $7 \times 7 \times 1$ for static electronic structure calculations of TMD monolayers, and $3 \times 3 \times 1$ for relaxation and static calculations of the Cr_2O_3 (0001) slab and heterostructures.

We found that there is a transfer of 0.36 electrons from chromia to the MoS_2 monolayer, but negligible charge transfer from chromia to a WSe_2 monolayer (0.04 electrons). In spite of the very small charge transfer, chromia induces a very high level of spin polarization in both a MoS_2 adlayer and a WSe_2 monolayer (Fig. 5). The take-away message is

that even for a large SOC system like the WSe_2 monolayer, the boundary polarization of chromia induces a high level of polarization. This means that for small source–drain bias voltages, the carriers that pass over the ME gate are of necessity, highly spin polarized. Simulations (Fig. 5) indicate an exchange splitting of ∼0.5 eV, in the vicinity of the valence band maximum and the Brillouin zone edge, due to interface polarization. This is more significant than the 150 meV expected for MoS_2, but in both cases the result of the very high spin polarization of the chromia boundary layer.

Induced polarization is evident in graphene on chromia [16], [77] but graphene is unsuitable in the devices presented here because of edge scattering, as noted above, and an absence of SOC. The density function theory results are much larger but still consistent with the observed exchange coupling of WSe_2 on the ferromagnet semiconductor CrI_3 [78].

V. CONCLUSION

There are multiple schemes for constructing a ME FET, and the nonvolatility of such a device can be enhanced by combining the ME with a channel with large SOC. Such devices, as described here have considerable added functionality. Some of these ME FET devices are spintronic devices, without ferromagnetism. Because there is no need to reverse the magnetization of any FM, even the most simple ME FET [17], [24] compares well with CMOS [87], with a comparable energy cost and reduced delay time. We acknowledge that materials other than chromia, exhibit ME switching, such as barium ferrite [88] and the rare earth ferrites [89] and these too, along with other like materials, could be used as the ME gate dielectric, in place of chromia, in the devices discussed here, so long as there is reliable isothermal switching at room temperature and above, at a low coercive voltage.

ACKNOWLEDGMENT

The authors would like to thank K. Wang for his technical assistance in the preparation of this paper.

REFERENCES

[1] C. Binek and B. Doudin, "Magnetoelectronics with magnetoelectrics," *J. Phys., Condens. Matter*, vol. 17, no. 2, pp. L39–L44, 2005.
[2] H. Dery, P. Dalal, L. Cywinski, and L. J. Sham, "Spin-based logic in semiconductors for reconfigurable large-scale circuits," *Nature*, vol. 447, pp. 573–576, May 2007.
[3] A. Ney, C. Pampuch, R. Koch, and K. H. Ploog, "Programmable computing with a single magnetoresistive element," *Nature*, vol. 425, no. 6957, pp. 485–487, 2003.
[4] D. E. Nikonov and I. A. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013.
[5] V. V. Zhirnov, J. A. Hutchby, G. I. Bourianoffls, and J. E. Brewer, "Emerging research logic devices," *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 37–46, May 2005.
[6] F. Jonietz *et al.*, "Spin transfer torques in MnSi at ultralow current densities," *Science*, vol. 330, pp. 1648–1651, Dec. 2010.
[7] W. Porod and M. Niemier, "Better computing with magnets—The simple bar magnet, shrunk down to the nanoscale, could be a powerful logic device," *IEEE Spectr.*, vol. 52, no. 9, pp. 44–60, Sep. 2015.
[8] X. He *et al.*, "Robust isothermal electric control of exchange bias at room temperature," *Nature Mater.*, vol. 9, pp. 579–585, Jun. 2010.
[9] W. Echtenkamp and C. Binek, "Electric control of exchange bias training," *Phys. Rev. Lett.*, vol. 111, no. 18, p. 187204, Oct. 2013.
[10] T. Ashida, M. Oida, N. Shimomura, T. Nozaki, T. Shibata, and M. Sahashi, "Isothermal electric switching of magnetization in Cr_2O_3/Co thin film system," *Appl. Phys. Lett.*, vol. 106, no. 13, p. 132407, Mar. 2015.
[11] T. Kosub, M. Kopte, F. Radu, O. G. Schmidt, and D. Makarov, "All-electric access to the magnetic-field-invariant magnetization of antiferromagnets," *Phys. Rev. Lett.*, vol. 115, p. 097201, Aug. 2015.
[12] T. Kosub *et al.*, "Purely antiferromagnetic magnetoelectric random access memory," *Nature Commun.*, vol. 8, Jan. 2017, Art. no. 13985.
[13] K. Toyoki *et al.*, "Magnetoelectric switching of perpendicular exchange bias in Pt/Co/a-Cr_2O_3/Pt stacked films," *Appl. Phys. Lett.*, vol. 106, p. 162404, Apr. 2015.
[14] N. Wu *et al.*, "Imaging and control of surface magnetization domains in a magnetoelectric antiferromagnet," *Phys. Rev. Lett.*, vol. 106, p. 087202, Feb. 2011.
[15] N. Wu and P. A. Dowben, "Magnetic surface states in high polarization materials," *Proc. SPIE*, vol. 8100, p. 81000T, Sep. 2011.
[16] R. Choudhary *et al.*, "Interface-induced spin polarization in graphene on chromia," *IEEE Magn. Lett.*, vol. 7, Feb. 2016, Art. no. 3101604.
[17] J. A. Kelber, C. Binek, P. A. Dowben, and K. Belashchenko, "Magneto-electric voltage controlled spin transistors," U.S. Patent 9 718 700, Aug. 1, 2017.
[18] Y. G. Semenov, K. W. Kim, and J. M. Zavada, "Spin field effect transistor with a graphene channel," *Appl. Phys. Lett.*, vol. 91, p. 153105, Oct. 2007.
[19] S. C. Stuart *et al.*, "Magnetoelectric oxide films for spin manipulation in graphene," *Phys. Status Solidi-Rapid Res. Lett.*, vol. 10, pp. 242–247, Mar. 2016.
[20] S. Manipatruni, D. E. Nikonov, and I. A. Young. (2015). "Spin-orbit logic with magnetoelectric nodes: A scalable charge mediated nonvolatile spintronic logic." [Online]. Available: http://arxiv.org/abs/1512.05428
[21] B. Doudin and C. Binek, "Magnetic spin valve with a magnetoelectric element," U.S. Patent 7 358 846, Apr. 15, 2008.
[22] M. Bibes and A. Barthélémy, "Multiferroics: Towards a magnetoelectric memory," *Nature Mater.*, vol. 7, no. 6, pp. 425–426, 2008.
[23] X. Chen, A. Hochstrat, P. Borisov, and W. Kleemann, "Magnetoelectric exchange bias systems in spintronics," *Appl. Phys. Lett.*, vol. 89, p. 202508, Nov. 2006.
[24] P. A. Dowben, C. Binek, and D. E. Nikonov, "Potential of nonvolatile magnetoelectric devices for spintronic applications," in *Nanoscale Silicon Devices*. Boca Raton, FL, USA: CRC Press, 2015, pp. 255–278.
[25] A. Jaiswal and K. Roy, "MESL: Proposal for a non-volatile cascadable magneto-electric spin logic," *Sci. Rep.*, vol. 7, Jan. 2017, Art. no. 39793.
[26] A. Jaiswal, I. Chakraborty, and K. Roy, "Energy-efficient memory using magneto-electric switching of ferromagnets," *IEEE Magn. Lett.*, vol. 8, Jun. 2017, Art. no. 4306905.
[27] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of nanoscale devices," *Proc. IEEE*, vol. 96, no. 9, pp. 1511–1550, Sep. 2008.
[28] D. E. Nikonov and I. A. Young, "Benchmarking spintronic logic devices based on magnetoelectric oxides," *J. Mater. Res.*, vol. 29, no. 18, pp. 2109–2115, Sep. 2014.
[29] D. E. Nikonov and I. A. Young, "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits," *IEEE J. Exploratory Solid-State Comput. Devices Circuits*, vol. 1, no. 1, pp. 3–11, Dec. 2015.
[30] N. Sharma, A. Marshall, J. Bird, and P. Dowben, "Magneto-electric magnetic tunnel junction as process adder for non-volatile memory applications," in *Proc. IEEE Dallas Circuits Syst. Conf. (DCAS)*, Oct. 2015, pp. 1–4.
[31] N. Sharma, A. Marshall, J. Bird, and P. Dowben, "Magneto-electric magnetic tunnel junction logic devices," in *Proc. 4th Berkeley Symp. Energy Efficient Electron. Syst. (E3S)*, Oct. 2015, pp. 1–3.
[32] N. Sharma, A. Marshall, J. Bird, and P. Dowben, "Multi-bit adder design using ME-MTJ technology," in *Proc. 11th Int. Conf. Adv. Semiconductor Devices Microsyst. (ASDAM)*, Nov. 2016, pp. 89–92.
[33] N. Sharma, A. Marshall, and J. Bird, "Verilog—A based compact model of a three-terminal ME-MTJ device," in *Proc. IEEE 16th Int. Conf. Nanotechnol. (IEEE-Nano)*, Aug. 2016, pp. 145–148.
[34] N. Sharma, A. Marshall, and P. Dowben, "Unipolar magnetoelectric magnetic tunnel junction (UMMTJ) devices and circuits," in *Proc. 17th IEEE Int. Conf. Nanotechnol. (IEEE NANO)*, Jul. 2017, pp. 861–865, doi: 10.1109/NANO.2017.8117352.

[35] N. Sharma, J. P. Bird, P. Dowben, and A. Marshall, "Compact-device model development for the energy-delay analysis of magneto-electric magnetic tunnel junction structures," *Semicond. Sci. Technol.*, vol. 31, p. 065022, Jun. 2016.

[36] N. Sharma, A. Marshall, and J. Bird, "Verilog—A compact model of a ME-MTJ based XNOR/NOR gate," in *Proc. IEEE 16th IEEE Int. Symp. Int. Conf. Nanotechnol. (IEEE-Nano)*, Jul. 2017, pp. 162–167.

[37] J. P. Velev, P. A. Dowben, E. Y. Tsymbal, S. J. Jenkins, and A. N. Caruso, "Interface effects in spin-polarized metal/insulator layered structures," *Surf. Sci. Rep.*, vol. 63, pp. 400–425, Sep. 2008.

[38] H. Liu, D. Bedau, D. Backes, J. A. Katine, J. Langer, and A. D. Kent, "Ultrafast switching in magnetic tunnel junction based orthogonal spin transfer devices," *Appl. Phys. Lett.*, vol. 97, no. 24, p. 242510, 2010.

[39] A. Iyama and T. Kimura, "Magnetoelectric hysteresis loops in Cr_2O_3 at room temperature," *Phys. Rev. B, Condens. Matter*, vol. 87, p. 180408, May 2013.

[40] J. Mathon, "Magnetisation of a strongly paramagnetic layer in contact with a ferromagnetic substrate," *J. Phys. F, Metal Phys.*, vol. 16, no. 9, p. L217, 1986.

[41] D. Schwenk, F. Fishman, and F. Schwabl, "Ferromagnetic multilayers: Statics and dynamics," *Phys. Rev. B, Condens. Matter*, vol. 38, no. 16, pp. 11618–11638, 1988.

[42] K. Hart and A. Slob, "Integrated injection logic: A new approach to LSI," *IEEE J. Solid-State Circuits*, vol. SSC-7, no. 5, pp. 346–351, Oct. 1972.

[43] Y. Lv *et al.* (2017). "Unidirectional spin Hall magnetoresistance in topological insulator/ferromagnetic layer heterostructures." [Online]. Available: https://arxiv.org/abs/1701.06505

[44] C. O. Avci, K. Garello, A. Ghosh, M. Gabureac, S. F. Alvarado, and P. Gambardella, "Unidirectional spin Hall magnetoresistance in ferromagnet/normal metal bilayers," *Nature Phys.*, vol. 11, pp. 570–575, Jul. 2015.

[45] M. D'yakonov and V. Perel, "Possibility of orienting electron spins with current," *Sov. J. Experim. Theor. Phys. Lett.*, vol. 13, p. 467, Jun. 1971.

[46] M. I. Dyakonov and V. I. Perel, "Current-induced spin orientation of electrons in semiconductors," *Phys. Lett. A*, vol. 35, no. 6, pp. 459–460, 1971.

[47] W. M. Saslow, "Spin Hall effect and irreversible thermodynamics: Center-to-edge transverse current-induced voltage," *Phys. Rev. B, Condens. Matter*, vol. 91, no. 1, p. 014401, 2015.

[48] Y. K. Kato, R. C. Myers, A. C. Gossard, and D. D. Awschalom, "Observation of the spin Hall effect in semiconductors," *Science*, vol. 306, no. 5703, pp. 1910–1913, 2004.

[49] S. O. Valenzuela and M. Tinkham, "Direct electronic measurement of the spin Hall effect," *Nature*, vol. 442, pp. 176–179, Jul. 2006.

[50] J. Wunderlich, B. Kaestner, J. Sinova, and T. Jungwirth, "Experimental observation of the spin-Hall effect in a two-dimensional spin-orbit coupled semiconductor system," *Phys. Rev. Lett.*, vol. 94, p. 047204, Feb. 2005.

[51] D. E. Nikonov, C. Binek, X. Hong, J. P. Bird, K. L. Wang, and P. A. Dowben, "Anti-ferromagnetic magneto-electric spin-orbit read logic," U.S. Patent Application No.: 62/460,164; filed February 17, 2017.

[52] M. Tosun *et al.*, "High-gain inverters based on WSe_2 complementary field-effect transistors," *ACS Nano*, vol. 8, no. 5, pp. 4948–4953, 2014.

[53] M. O. Li, D. Esseni, J. J. Nahas, D. Jena, and H. G. Xing, "Two-dimensional heterojunction interlayer tunneling field effect transistors (thin-TFETs)," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 200–207, May 2015.

[54] D. E. Nikonov, G. I. Bourianoff, G. Rowlands, and I. N. Krivorotov, "Strategies and tolerances of spin transfer torque switching," *J. Appl. Phys.*, vol. 107, p. 113910, Jun. 2010.

[55] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nano*, vol. 6, pp. 147–150, Mar. 2011.

[56] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered WSe_2 p-FETs with chemically doped contacts," *Nano Lett.*, vol. 12, pp. 3788–3792, Jun. 2012.

[57] G. Schmidt, D. Ferrand, L. W. Molenkamp, A. T. Filip, and B. J. van Wees, "Fundamental obstacle for electrical spin injection from a ferromagnetic metal into a diffusive semiconductor," *Phys. Rev. B, Condens. Matter*, vol. 62, pp. R4790–R4793, Aug. 2000.

[58] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proc. IEEE*, vol. 101, no. 7, pp. 1585–1602, Jul. 2013.

[59] J. Kang, W. Cao, X. J. Xie, D. Sarkar, W. Liu, and K. Banerjee, "Graphene and beyond-graphene 2D crystals for next-generation green electronics," *Proc. SPIE*, vol. 9083, p. 908305, Jun. 2014.

[60] X. Blase *et al.*, "Conductance of functionalized nanotubes, graphene and nanowires: From *ab initio* to mesoscopic physics," *Phys. Status Solidi B*, vol. 247, pp. 2962–2967, Dec. 2010.

[61] V. K. Dugaev and M. I. Katsnelson, "Edge scattering of electrons in graphene: Boltzmann equation approach to the transport in graphene nanoribbons and nanodisks," *Phys. Rev. B, Condens. Matter*, vol. 88, no. 23, p. 235432, 2013.

[62] E. R. Mucciolo and C. H. Lewenkopf, "Disorder and electronic transport in graphene," *J. Phys., Condens. Matter*, vol. 22, no. 27, p. 273201, 2010.

[63] M. Wimmer, I. Adagideli, S. Berber, D. Tománek, and K. Richter, "Spin currents in rough graphene nanoribbons: Universal fluctuations and spin injection," *Phys. Rev. Lett.*, vol. 100, p. 177207, May 2008.

[64] J. Wurm, K. Richter, and I. Adagideli, "Edge effects in graphene nanostructures: From multiple reflection expansion to density of states," *Phys. Rev. B, Condens. Matter*, vol. 84, p. 075468, Aug. 2011.

[65] O. V. Yazyev, "Emergence of magnetism in graphene materials and nanostructures," *Rep. Progr. Phys.*, vol. 73, no. 5, p. 056501, 2010.

[66] M. Y. Han, J. C. Brant, and P. Kim, "Electron transport in disordered graphene nanoribbons," *Phys. Rev. Lett.*, vol. 104, p. 056801, Feb. 2010.

[67] S. A. Jensen *et al.*, "Ultrafast photoconductivity of graphene nanoribbons and carbon nanotubes," *Nano Lett.*, vol. 13, pp. 5925–5930, Nov. 2013.

[68] Y.-J. Shi, J. Lan, E.-J. Ye, W.-Q. Sui, and X. Zhao, "Four-terminal impedance of a graphene nanoribbon based structure," *Eur. Phys. J. B*, vol. 87, p. 251, Oct. 2014.

[69] J. Dai and X. C. Zeng, "Titanium trisulfide monolayer: Theoretical prediction of a new direct-gap semiconductor with high and anisotropic carrier mobility," *Angew. Chem.*, vol. 54, pp. 7572–7576, Jun. 2015.

[70] N. Benramdane and R. H. Misho, "Structural and optical properties of In_4Se_3 thin films obtained by flash evaporation," *Solar Energy Mater. Solar Cells*, vol. 37, pp. 367–377, Jul. 1995.

[71] Y. B. Losovyj *et al.*, "The electronic structure of surface chains in the layered semiconductor $In_4Se_3(100)$," *Appl. Phys. Lett.*, vol. 92, no. 12, p. 122107, 2008.

[72] K. Fukutani *et al.*, "High-resolution angle-resolved photoemission study of quasi-one-dimensional semiconductor In_4Se_3," *J. Phys. Soc. Jpn.*, vol. 84, p. 074710, Jun. 2015.

[73] Y. S. Lim *et al.*, "Condenson state and its effects on thermoelectric properties in In_4Se_3," *J. Phys. D, Appl. Phys.*, vol. 46, no. 27, p. 275304, 2013.

[74] V. P. Savchin, "Characteristics of the transport properties of layer In_4Se_3 crystals," *Sov. Phys. Semiconduct.-USSR*, vol. 15, p. 827, 1981.

[75] A. Lipatov, P. M. Wilson, M. Shekhirev, J. D. Teeter, R. Netusil, and A. Sinitskii, "Few-layered titanium trisulfide (TiS_3) field-effect transistors," *Nanoscale*, vol. 7, pp. 12291–12296, Jun. 2015.

[76] M. Neupane *et al.*, "Observation of quantum-tunnelling-modulated spin texture in ultrathin topological insulator Bi_2Se_3 films," *Nature Commun.*, vol. 5, May 2014, Art. no. 3841.

[77] S. Cao *et al.*, "Moving towards the magnetoelectric graphene transistor," *Appl. Phys. Lett.*, vol. 111, p. 182402, Oct. 2017.

[78] D. Zhong *et al.*, "Van der Waals engineering of ferromagnetic semiconductor heterostructures for spin and valleytronics," *Sci. Adv.*, vol. 3, no. 5, p. e1603113, 2017.

[79] G. Kresse and J. Hafner, "*Ab initio* molecular dynamics for liquid metals," *Phys. Rev. B, Condens. Matter*, vol. 47, no. 1, pp. 558–561, 1993.

[80] G. Kresse and J. Hafner, "*Ab initio* molecular-dynamics simulation of the liquid-metal-amorphous-semiconductor transition in germanium," *Phys. Rev. B, Condens. Matter*, vol. 49, pp. 14251–14269, May 1994.

[81] J. P. Perdew, K. Burke, and M. Ernzerhof, "Generalized gradient approximation made simple," *Phys. Rev. Lett.*, vol. 77, pp. 3865–3868, Oct. 1996.

[82] J. Klimes, D. R. Bowler, and A. Michaelides, "Chemical accuracy for the van der Waals density functional," *J. Phys., Condens. Matter*, vol. 22, p. 022201, Dec. 2009.

[83] J. Klimeš, D. R. Bowler, and A. Michaelides, "Van der Waals density functionals applied to solids," *Phys. Rev. B, Condens. Matter*, vol. 83, p. 195131, May 2011.

[84] G. Makov and M. C. Payne, "Periodic boundary conditions in *ab initio* calculations," *Phys. Rev. B, Condens. Matter*, vol. 51, pp. 4014–4022, Feb. 1995.

[85] J. Neugebauer and M. Scheffler, "Adsorbate-substrate and adsorbate-adsorbate interactions of Na and K adlayers on Al (111)," *Phys. Rev. B, Condens. Matter*, vol. 46, pp. 16067–16080, Dec. 1992.

[86] H. J. Monkhorst and J. D. Pack, ''Special points for Brillouin-zone integrations,'' *Phys. Rev. B, Condens. Matter*, vol. 13, pp. 5188–5192, Jun. 1976.
[87] N. Sharma, A. Marshall, J. Bird, and P. Dowben, ''Verilog—A based compact modeling of the ME-FET device,'' in *Proc. E3S Symp. Steep Transistors Workshop*, 2017.
[88] J. T. Heron *et al.*, ''Electric-field-induced magnetization reversal in a ferromagnet-multiferroic heterostructure,'' *Phys. Rev. Lett.*, vol. 107, p. 217202, Nov. 2011.
[89] Y. Tokunaga, Y. Taguchi, T. H. Arima, and Y. Tokura, ''Electric-field-induced generation and reversal of ferromagnetic moment in ferrites,'' *Nature Phys.*, vol. 8, pp. 838–844, Aug. 2012.

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