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Interface characterization of atomic layer deposited high-k on non-polar GaN

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The interface properties between dielectrics and semiconductors are crucial for electronic devices. In this work, we report the electrical characterization of the interface properties between atomic layer deposited Al_2O_3 and HfO_2 on non-polar a-plane $(11\bar{2}0)$ and m-plane $(1\bar{1}00)$ GaN grown by hybrid vapor phase epitaxy. A metal oxide semiconductor capacitor (MOSCAP) structure was used to evaluate the interface properties. The impact of annealing on the interface properties was also investigated. The border trap in the oxide, characterized by the capacitance-voltage (C-V) hysteresis loop, was low. The interface state density (D_{it}), extracted using the ac conductance method, is in the range of $0.5 \times 10^{12}/cm^2$ eV to $7.5 \times 10^{11}/cm^2$ eV within an energy range from 0.2 eV to 0.5 eV below the conduction band minimum. The m-plane GaN MOSCAPs exhibited better interface properties than the a-plane GaN MOSCAPs after annealing. Without annealing, Al_2O_3 dielectrics had higher border trap density and interface state density compared to HfO_2 dielectrics. However, the annealing had different impacts on Al_2O_3 dielectrics as compared to HfO_2. Our results showed that the annealing degraded the quality of the interface in HfO_2, but it improved the quality of the interface in Al_2O_3 devices. The annealing also reduced the positive trapped oxide charge, resulting in a shift of C-V curves towards the positive bias region. *Published by AIP Publishing.*
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I. INTRODUCTION

GaN, a wide bandgap semiconductor, has been extensively studied for a variety of applications such as power amplifiers, power conversion devices, and light-emitting diodes (LEDs) because of its large bandgap, high electron mobility, high electron velocity, high breakdown voltage, and the capability of forming various alloys.[1–5] GaN is a polar material with a wurtzite crystal structure, which results in a large polarization field along the *c*-axis of the crystal[6,7] which is the traditional direction of the GaN crystal growth. The polarization field has been used for polarization doping of heterostructures that show high electron mobilities.[8,9] The polarization field has been exploited to increase the hole density in the p-type AlGaN/GaN heterojunction.[10] However, for optoelectronic devices, the separation of electron and hole wavefunctions due to the polarization field leads to a reduction of the radiative emission rate.[4,7,11] Moreover, the p-type doping flexibility is reduced in polar GaN because of the polarity inversion caused by the high Mg flux for achieving a high Mg concentration.[12–14] In recent years, novel non-polar GaN has drawn a lot of attention for optoelectronic and electronic devices.[15–18] Unlike the conventional polar GaN, the polarization field is absent in the non-polar GaN crystal along the non-polar direction.[7,19] The absence of the polarization field in non-polar GaN benefits both optoelectronic and electronic devices.[20,21] Non-polar optoelectronic device performance has been greatly improved as compared to that of polar optoelectronics devices, with reduction of the efficiency droop.[11,22,23] The density function theory (DFT) predicts that the Fermi level in p-type non-polar GaN is unpinned,[24] which could reduce the contact resistance to p-type GaN.[14] We have previously reported that the Fermi level in n-type non-polar m-plane GaN was pinned close to mid-gap (~2.4 eV above the valence band maximum).[25] The low contact resistance to p-type GaN is beneficial to heterostructure bipolar transistors (HBTs) and p-channel devices.[26,27] A normally off p-type semi-polar GaN power device with high breakdown voltage was demonstrated,[28] which can also benefit from the low contact resistance to p-type GaN.

Dielectrics are used as the gate barrier and passivation layer in electronic devices. It is important to quantitatively understand the interface electrical properties between the dielectric layer and non-polar GaN for electronic applications. Atomic layer deposition (ALD) has been widely used for depositing a low interface state density high-k gate dielectric layer on silicon, III-V materials, and emerging 2D materials.[10,29–33] The interface properties of ALD-dielectric/polar GaN in terms of interface state density (D_{it}) have been studied by the photo-assisted capacitance-voltage (CV) technique,[34] the conductance method,[34,35] and deep-level transient spectroscopy.[36] The impact of thermal annealing on the interface properties has also been investigated.[34] However, there is no report on the interface properties between dielectrics and non-polar GaN. The band offsets between ALD-Al_2O_3 and m-plane GaN characterized by x-ray photoelectron spectroscopy have been reported,[25] including the structural characterization. In this work, we evaluated the interface state density and border trap density in ALD deposited high-k dielectrics on a-plane and m-plane non-polar GaN.

II. EXPERIMENT DETAILS

The non-polar *a*-plane and *m*-plane bulk GaN wafers were prepared at Kyma technologies Inc. The non-polar GaN substrates were sliced from polar *c*-plane GaN which

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was grown by hybrid vapor phase epitaxy (HVPE). The root mean square (rms) roughness of the a-plane and m-plane GaN substrates was 0.3 nm and 0.5 nm, respectively. The van der Pauw Hall measurement gave an n-type conductivity with a doping density of $\sim 1 \times 10^{16}/\text{cm}^3$ for both samples. The metal-oxide-semiconductor (MOSCAP) structures were fabricated to study the interface properties. It is necessary to form ohmic contacts to GaN in order to study the frequency dependent capacitance-voltage profiles. It has been reported that the contact resistance to GaN can be reduced by reactive ion etching and post deposition annealing.[37] The MOSCAP structure is shown in Fig. 1(a). After standard solvent and HF cleaning, the wafers were exposed to an inductively coupled plasma reactive ion etcher (ICP-RIE) with a gas mixture of BCl_3 and Cl_2.[25] The Ti/Al/Ni/Au bottom ohmic contact was patterned by electron-beam lithography (EBL) and the lift-off process. Next, the wafers were subjected to a rapid thermal annealing (RTA) process at 950 °C for 1 min in N_2 ambient. Afterwards, the high-k dielectric layer was deposited using a thermal ALD tool. Here, we investigated two high-k dielectrics, Al_2O_3 and HfO_2. Al_2O_3 was deposited at 300 °C with trimethylaluminum (TMA) and H_2O. HfO_2 was deposited at 150 °C with tetrakis(dimethylamido)hafnium (TDMAH) and H_2O. A top gate contact was formed by EBL and the lift-off process. The bottom contact was opened by an alumina etchant for Al_2O_3-MOSCAPs and dilute HF for HfO_2-MOSCAPs. To investigate the impacts of annealing on the interface properties, the Al_2O_3-MOSCAPs were annealed in N_2 ambient at 500 °C for 1 min, while the HfO_2-MOSCAPs were annealed in vacuum at 350 °C for 1 min.

The capacitance of the MOSCAPs was measured using an Agilent 4294A precise impedance analyzer with a HP42941 impedance probe. Border traps that are close to the interface of dielectric/GaN can respond to the Fermi level and affect the device performance. The border trap density ($N_{bt,tot}$) is calculated from the capacitance-voltage (C-V) hysteresis loop by the following equation:[34]

$$N_{bt,tot} = \frac{1}{qA}\int_{V_1}^{V_2} |C_{up} - C_{dwn}| dV, \tag{1}$$

where V is the applied bias, q is the charge unit, A is the device area, and C_{up} and C_{dwn} are the measured capacitances when the bias is swept from the negative to the positive region and vice versa. The interface state density (D_{it}) is calculated using the conductance method which exploits the change in occupancy of interface states.[35] Using the parallel conductance model, D_{it} can be estimated by the following equation:[35]

$$D_{it} = \frac{2.5}{qA}\left(\frac{G_p}{\omega}\right)_{max}, \tag{2}$$

where ω is the probing frequency in rad/s. The parallel conductance, (G_p/ω), can be calculated from the measured capacitance (C_m) and conductance (G_m) directly by the ignoring series resistance[38]

$$\frac{\langle G_p \rangle}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{3}$$

where C_{ox} is the oxide capacitance. Since the change in occupancy only occurs when the energy of interface states is close to the Fermi level, the relative energy level (ΔE) of the interface states can be found by the SRH model[35]

$$\Delta E = k_B T \ln(\tau \sigma v_t N_c), \tag{4}$$

where k_B is the Boltzmann constant, T is the temperature, τ is the lifetime of the interface states, σ is the capture cross section of the interface states, v_t is the thermal velocity, and N_c is the effective density of state in the conduction band.

III. RESULTS AND DISCUSSION

A. Al_2O_3/m-plane GaN MOSCAP

Figures 2(a) and 2(b) show the high frequency (1 MHz) C-V hysteresis loop of the Al_2O_3/m-plane GaN MOSCAP measured at 1 MHz before and after annealing. The inset shows the distribution of the border traps as a function of gate bias. After annealing, there was a positive shift of the C-V curve, which indicated a reduction of positive trapped oxide charge. The total density of border traps reduced from $1.8 \times 10^{11}/\text{cm}^2$ to $0.86 \times 10^{11}/\text{cm}^2$ with annealing. Figures 3(a) and 3(b) show the frequency-dependent C-V profiles before and after annealing. The C-V curves were measured from 10 kHz to 1 MHz. In the negative bias region, only marginal frequency dispersion was observed, indicating a low D_{it}. However, after annealing, a relatively larger dispersion was observed when the gate bias was positive, as shown in Fig. 3(b). Therefore, we could expect a high D_{it} in the positive gate bias region. The knowledge of C_{ox} was required to extract D_{it}; however, we were unable to measure

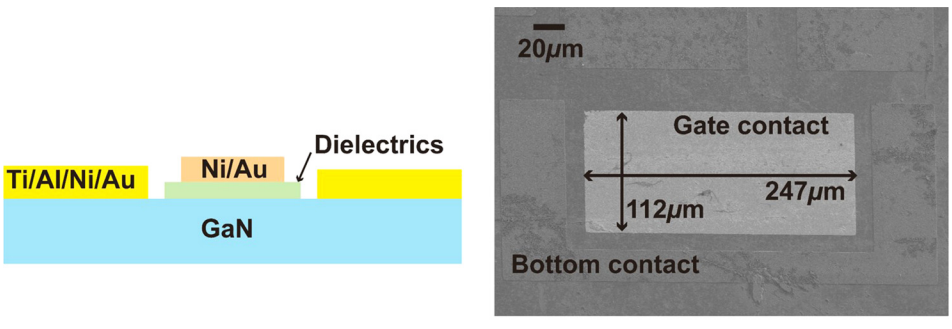

FIG. 1. (a) Schematic cross section of a MOSCAP. (b) SEM image of the fabricated device.

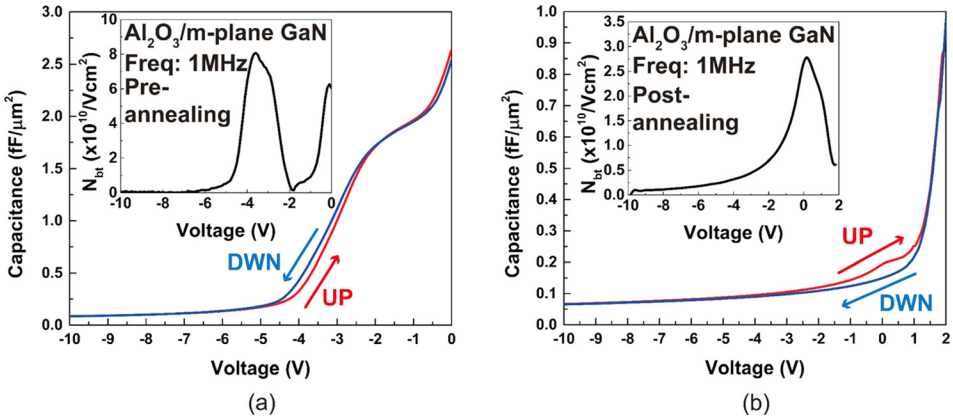

FIG. 2. C-V hysteresis loop of the Al_2O_3/m-plane GaN device (a) before annealing and (b) after annealing. The insets show the distribution of the border traps as a function of gate bias. After annealing, the C-V curves shifted towards the positive bias region. Reprinted with permission from Y. Jia *et al.*, Phys. Status Solidi B **254**, 1600681 (2017). Copyright 2017 John Wiley and Sons.

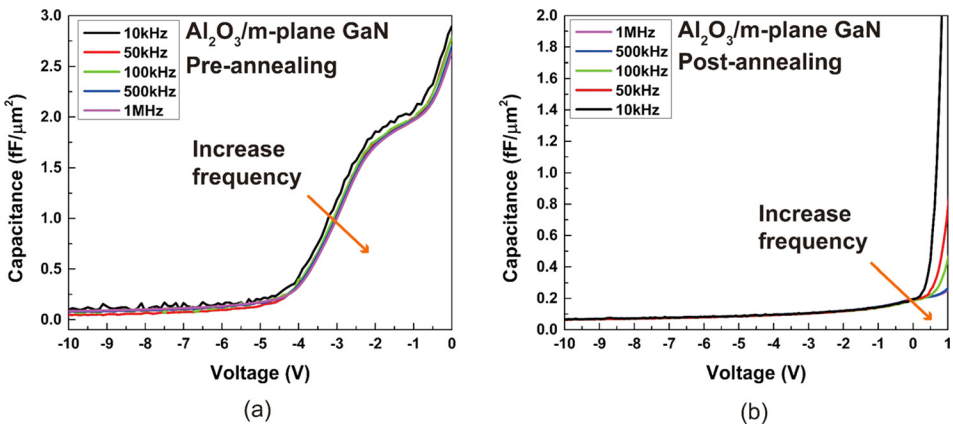

FIG. 3. Frequency-dependent C-V curves of the Al_2O_3/m-plane GaN device (a) before annealing and (b) after annealing. A small frequency dispersion was observed at negative bias. Reprinted with permission from Y. Jia *et al.*, Phys. Status Solidi B **254**, 1600681 (2017). Copyright 2017 John Wiley and Sons.

it directly from the GaN MOSCAPs due to the high leakage current in the accumulation region, so we assumed that the C_{ox} of GaN devices would be the same as that of Si devices that were fabricated simultaneously. Figure 4(a) shows the calculated conductance peaks (G_p/ω) as a function of frequency using Eq. (3). The G_p/ω peaks were measured from -2 V to -10 V. It can be seen that when the bias was small (-2 V to -5 V), the peak was modulated by the gate bias. The peak shifted to lower frequency with the increasing gate bias. When the gate bias was sufficiently large, the peak was pinned at $\sim$200 Hz. The pinning of the G_p/ω peaks can be attributed to the bulk traps. Figure 4(b) shows the calculated conductance peak as a function of frequency after annealing. As indicated in Fig. 3, because the C-V curves shifted to the positive bias region after annealing, the G_p/ω peaks after annealing were measured from $+2$ V to -2 V. Similar to the G_p/ω peak before annealing, the conductance peak was modulated by bias. The peak shifted from 6 MHz to 400 Hz when the bias changed from 2 V to 0 V. When the bias moved to the negative region, the peak shifted to a very low frequency which was outside of the measurable range of the instrument at room temperature. Figure 5 shows the calculated D_{it} as a function of its energy level using Eq. (4) before and after annealing. Before annealing, D_{it} ranged from $\sim 2.5 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ to $\sim 5.0 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ and its energy ranged from 0.51 eV to 0.46 eV. Our reported D_{it} values were slightly higher than the D_{it} of Al_2O_3/c-plane GaN reported by Winzer *et al.*[34] in the comparable energy range. After annealing, D_{it} was in the range of $2.0 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ to $2.5 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ and E_{it} was closer to conduction band minimum (CBM) compared to before annealing. At an E_{it} of greater than 0.45 eV, D_{it} decreased from $5 \times 10^{12}\,\mathrm{cm^{-2}V^{-1}}$ after annealing.

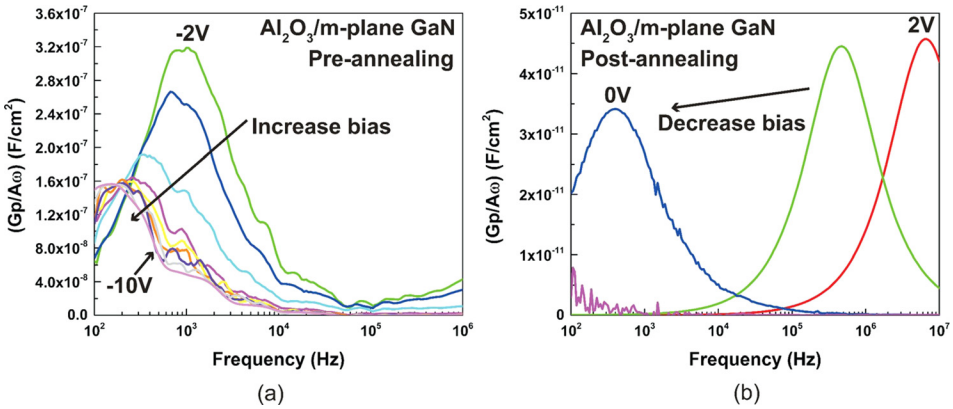

FIG. 4. G_p/ω peak of the Al_2O_3/m-plane GaN device (a) before annealing and (b) after annealing. The peak was modulated by bias. The peaks were pinned at $\sim$200 Hz when the bias was greater than -5 V.

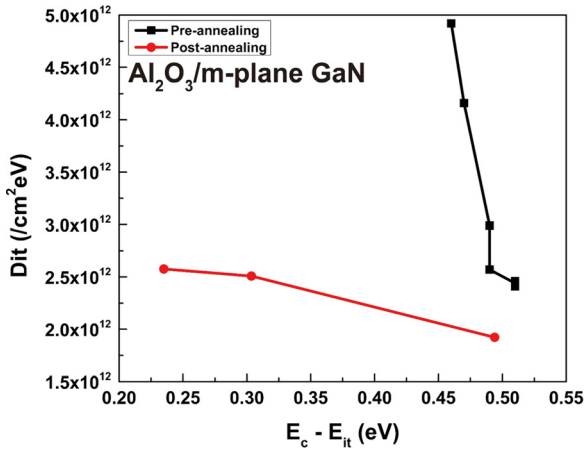

FIG. 5. The calculated D_{it} of Al_2O_3/m-plane GaN devices before and after annealing. D_{it} was found to be in the range of $2.5 \times 10^{12}/cm^2$ eV to $5.0 \times 10^{12}/cm^2$ eV without annealing. The annealing process reduced D_{it}.

B. HfO_2/m-plane GaN MOSCAP

Figures 6(a) and 6(b) show the C-V hysteresis loop of the HfO_2/m-plane GaN MOSCAP measured at 1 MHz before and after annealing. Similar to the Al_2O_3/m-plane GaN MOSCAPs, there was a positive shift in the C-V curve after annealing. The inset shows the calculated distribution of border traps as a function of gate bias. The border trap density was calculated to be $1.0 \times 10^{11}/cm^2$ before annealing and $1.9 \times 10^{11}/cm^2$ after annealing. The annealing process slightly increased the density of border traps. Figures 7(a) and 7(b) show the frequency-dependent C-V profiles measured from 1 kHz to 1 MHz pre- and post-annealing. Similar to Al_2O_3/m-plane GaN MOSCAPs, a small frequency dispersion in C-V curves was observed before annealing. After annealing, C-V curves showed a large dispersion in the positive gate bias region, indicating a high D_{it}. Figures 8(a) and 8(b) show the G_p/ω peaks as a function of frequency before and after annealing. In Fig. 8(a), it can be seen that the position of the G_p/ω peak at a gate bias of 1 V was higher than 10 MHz which exceeded the measurement capability and a partial peak was observed. While the position of the G_p/ω peak at a gate voltage of −1 V was lower than the lower limit of the measurement frequency (100 Hz not shown). Only one clear G_p/ω peak was observed at a bias of 0 V, which suggested that the interface states were close to CBM and mid-gap. Similarly, in Fig. 8(b), after annealing, there was no clear or complete G_p/ω peak when the bias became negative. Figure 9 shows the calculated D_{it} before and after annealing within the measurable range. Before annealing, D_{it} was about $2.5 \times 10^{12}/cm^2\ eV^{-1}$ to $0.7 \times 10^{12}/cm^2\ eV^{-1}$ at an E_{it} in the range of 0.23–0.25 eV. As we mentioned above, the interface states were close to CBM. After annealing, D_{it} increased to $\sim 7.5 \times 10^{12}/cm^2$ eV at an E_{it} of 0.28 eV and $\sim 6.5 \times 10^{12}/cm^2$ eV at an E_{it} of 0.35 eV. The annealing process increased D_{it}. The effect of annealing on HfO_2-MOSCAPs was opposite to that of on Al_2O_3-MOSCAPs. It should be noted that a temperature dependent conductance measurement is necessary to probe more of the interface states because at room temperature the measurable range of E_{it} is limited.

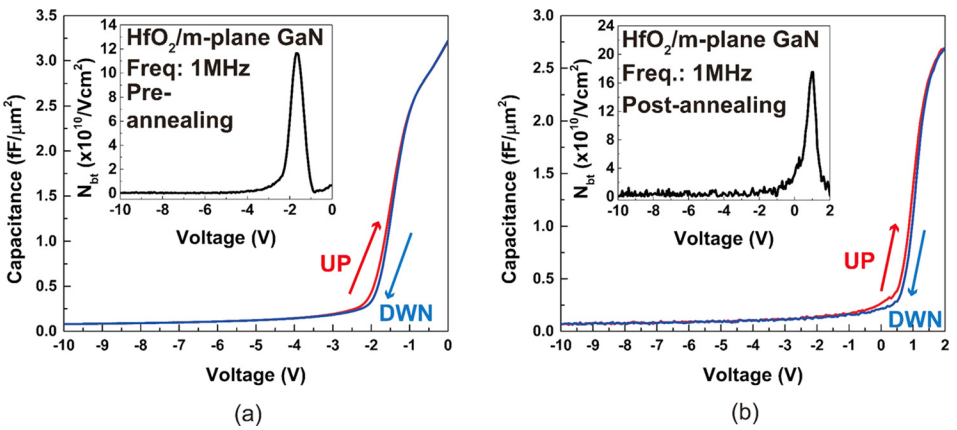

FIG. 6. C-V hysteresis loop of the HfO_2/m-plane GaN device (a) before annealing and (b) after annealing. The insets show the distribution of the border traps as a function of gate bias. After annealing, the C-V curves shifted towards the positive bias region.

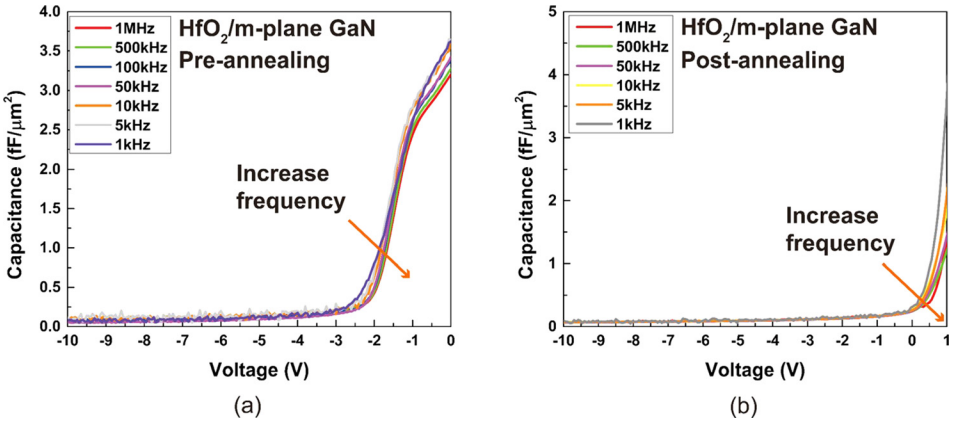

FIG. 7. Frequency-dependent C-V curves of the HfO_2/m-plane GaN device (a) before annealing and (b) after annealing. A small frequency dispersion was observed at negative bias.

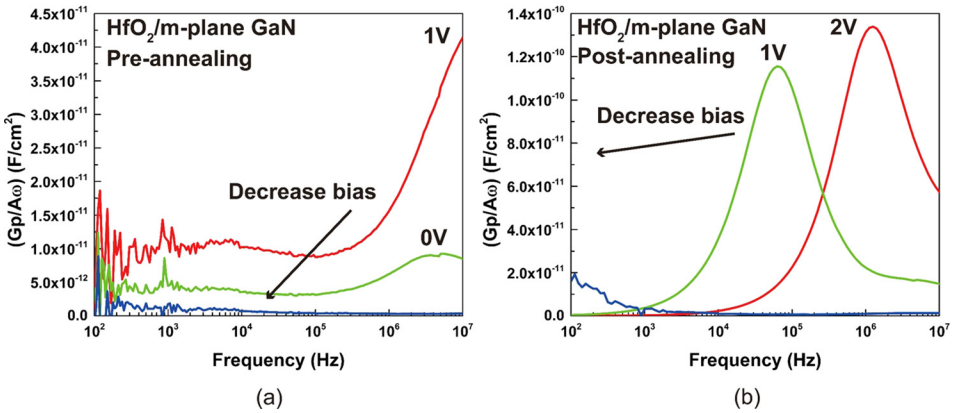

FIG. 8. G_p/ω peak of the HfO_2/m-plane GaN device (a) before annealing and (b) after annealing. The peak was modulated by bias. Only two peaks were observed before and after annealing.

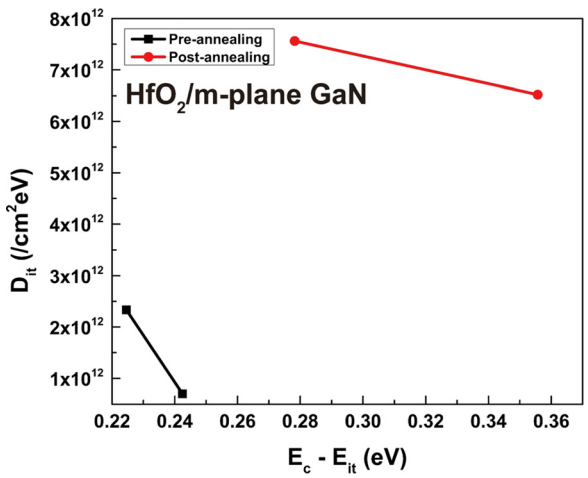

FIG. 9. The calculated D_{it} of HfO_2/m-plane GaN devices before and after annealing. D_{it} was found to be in the range of $6 \times 10^{11}/cm^2$ eV to $2.5 \times 10^{12}/cm^2$ eV without annealing. The annealing process increased D_{it}.

C. Al_2O_3/a-plane GaN MOSCAP and HfO_2/a-plane GaN MOSCAP

Unlike the m-plane GaN MOSCAPs, the a-plane GaN MOSCAPs were characterized after the annealing process because the MOSCAPs showed a high gate leakage current before annealing. The devices were subjected to the same annealing condition as m-plane GaN MOSCAPs. Figures 10(a) and 10(b) show the C-V hysteresis loop of the Al_2O_3/a-plane GaN MOSCAP and HfO_2/a-plane GaN MOSCAP, respectively. The insets show the corresponding border trap distribution as a function of gate bias. In Fig. 10(a), it can be seen that a slightly large dispersion was observed, indicating a high N_{bt} inside the oxide. The C-V curves in the large negative bias region did not show a depletion behavior, which could be attributed to the high density of interface states and/or oxide traps. In contrast, in Fig. 10(b), the HfO_2/a-plane GaN MOSCAP showed a flat C-V curve in the large negative bias region. However, its C-V hysteresis loop exhibited a large dispersion between gate biases of 1 V and −3 V, indicating a high N_{bt}. The inset of Fig. 10(a) showed a very broad distribution of N_{bt}, giving an $N_{bt,\ tot}$ of $2.7 \times 10^{11}/cm^2$, whereas the inset of Fig. 10(b) showed a narrow distribution of N_{bt}. However, the peak reached a high value of $2.5 \times 10^{11}/cm^2$, resulting in a total $N_{bt,\ tot}$ of $4.3 \times 10^{11}/cm^2$. Figures 11(a) and 11(b) show the frequency-dependent C-V curves of Al_2O_3/a-plane GaN and HfO_2/a-plane GaN MOSCAPs after annealing. The measured frequencies for the Al_2O_3/a-plane GaN MOSCAP were from 50 kHz to 1 MHz and for the HfO_2/a-plane GaN MOSCAP were from 1 kHz to 1 MHz. The bias of the Al_2O_3/a-plane GaN MOSCAP was swept from 1 V to −5 V due to high leakage current at low frequency. In Fig. 11(a), we can see that there was a large frequency dispersion in the negative bias region, suggesting a high D_{it}. However, the HfO_2/a-plane GaN MOSCAP revealed large dispersion in the positive bias region. Figures 12(a) and 12(b) show the G_p/ω peaks of Al_2O_3/a-plane GaN and HfO_2/a-plane GaN MOSCAPs. In Fig. 12(a), when the bias was greater than 1 V, the peak located at a frequency of >10 MHz. With decreasing bias to the negative region, the peak shifted to lower frequency and it was pinned at ∼300 Hz when the bias was greater than −2 V. Figure 12(b)

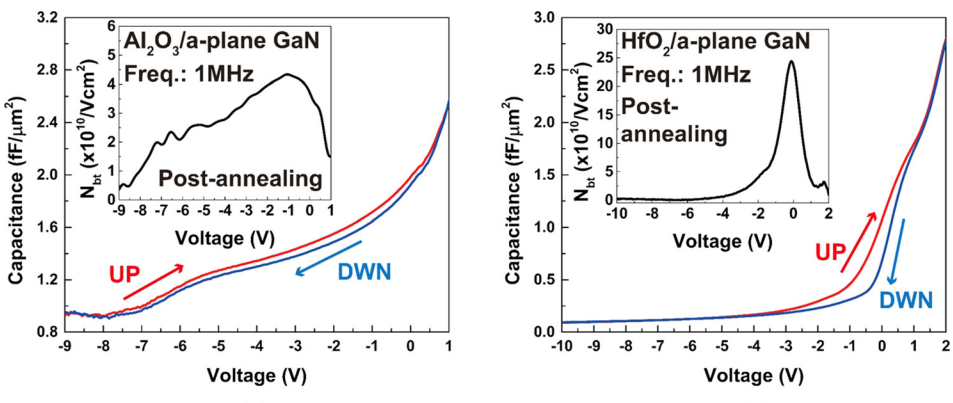

FIG. 10. C-V hysteresis loop of (a) the Al_2O_3/a-plane GaN device and (b) HfO_2/a-plane GaN device after annealing. The insets show the distribution of border traps as a function of bias. $N_{bt,\ tot}$ was higher than that of the m-plane GaN device.

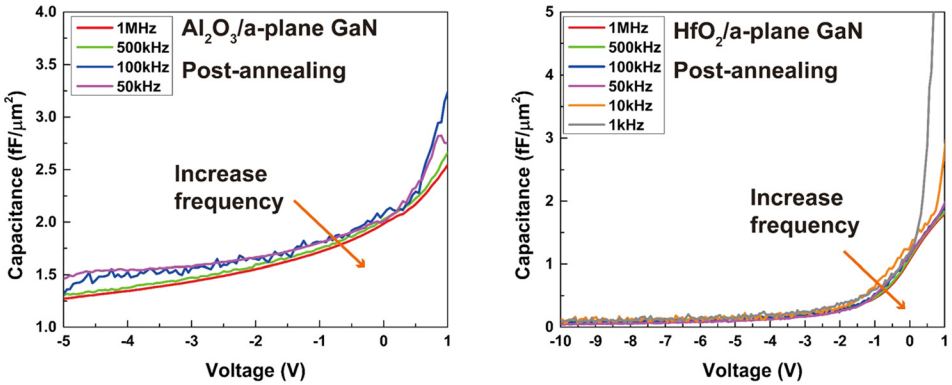

FIG. 11. Frequency-dependent C-V curves of (a) the Al_2O_3/a-plane GaN device and (b) HfO_2/a-plane GaN device after annealing. The Al_2O_3/a-plane GaN device showed relatively large frequency dispersion compared to the HfO_2/a-plane GaN device in the negative bias region.

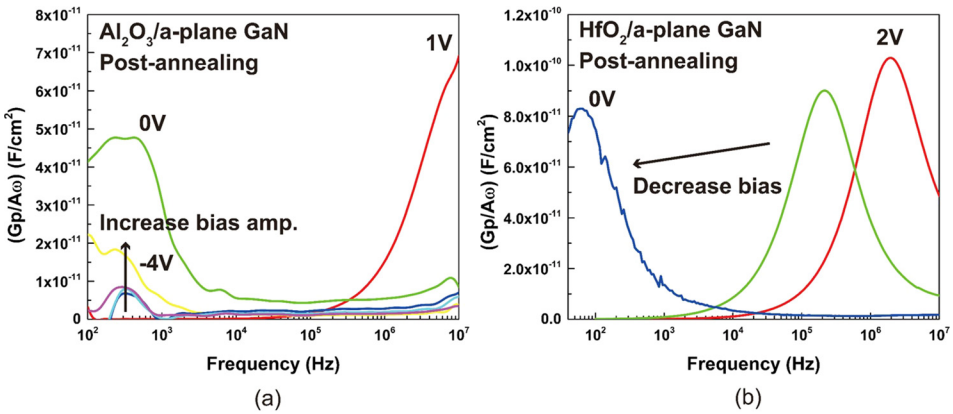

FIG. 12. G_p/ω peak of (a) the Al_2O_3/a-plane GaN device and (b) HfO_2/m-plane GaN device after annealing. The peak was modulated by bias. The G_p/ω peak was pinned at ~200 Hz probably caused by bulk trap loss when bias was greater than −1 V.

clearly shows voltage modulated G_p/ω peaks from 2 V to 0 V. However, when the bias was in the negative region, the G_p/ω peak was out of the measurable range. Figure 13 shows the calculated D_{it} of the MOSCAPs. The D_{it} of the Al_2O_3/GaN device was $>8.5 \times 10^{12}/cm^2$ eV at an E_{it} of 0.23 eV and $\sim 1.2 \times 10^{12}/cm^2$ eV at an E_{it} of 0.48 eV. When the gate bias changed from −2 V to −4 V, D_{it} increased from $\sim 1.2 \times 10^{12}/cm^2$ eV to $\sim 4 \times 10^{12}/cm^2$ eV. The D_{it} of the HfO_2/GaN device changed from $7.6 \times 10^{12}/cm^2$ to $6.2 \times 10^{12}/cm^2$ eV within the energy range from 0.25 eV to 0.51 eV. Both Al_2O_3/a-plane GaN and HfO_2/a-plane GaN devices exhibited comparable interface characteristics.

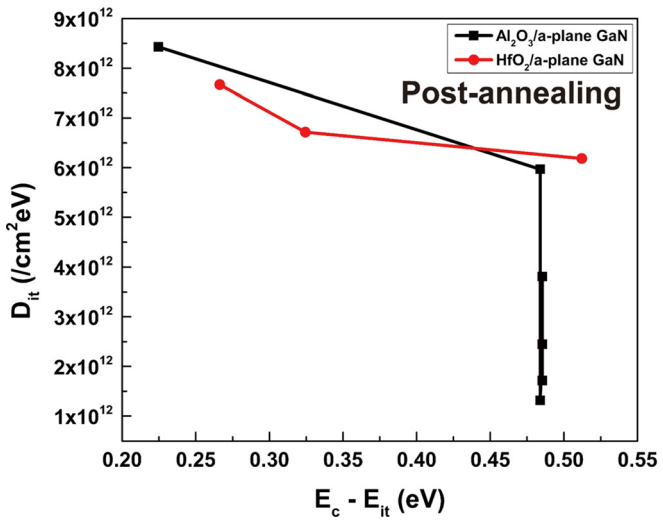

FIG. 13. The calculated D_{it} of the Al_2O_3/m-plane GaN device and (b) HfO_2/m-plane GaN device after annealing. In terms of D_{it}, both devices had comparable performance.

A summary of the characterization results is given in Table I. For the device with Al_2O_3 as a dielectric layer, the annealing process was beneficial to the reduction of $N_{bt,\ tot}$ inside the oxide and D_{it} at the interface. In contrast, the annealing process, however, degenerated the interface of HfO_2/GaN devices by increasing $N_{bt,\ tot}$ and D_{it}. However, we need to note that the inadequate annealing process might also contribute to this degeneration. In addition, the annealing process removed the positive oxide charge, leading to a shift of the C-V curve towards the positive bias region. By comparing the polarity of GaN substrates, the a-plane GaN MOSCAPs always exhibited higher $N_{bt,\ tot}$ and D_{it} than m-plane GaN MOSCAPs. Before annealing, HfO_2 grown on GaN had the lowest D_{it}. If the device was subjected to annealing, Al_2O_3 grown on GaN could offer better quality of the interface. From these four devices, we can see that at room temperature, the lowest E_{it} was close to ~0.5 eV below the CBM. This value was comparable to the DFT model, which is ~0.7 eV below CBM for m-plane GaN and ~0.5 eV for a-plane GaN.[24] Compared with the $N_{bt,\ tot}$ of Al_2O_3/c-plane GaN reported by Winzer *et al.*,[34] our Al_2O_3/m-plane GaN MOSCAPs showed low $N_{bt,\ tot}$, but it could be partially attributed to the voltage sweeping range because of the incapability of obtaining C-V curves at large positive bias due to the high leakage current.

TABLE I. Summary of the electrical characterization.

Device	Al_2O_3/m-plane GaN		HfO_2/m-plane GaN		Al_2O_3/a-plane GaN	HfO_2/a-plane GaN
Annealing	Pre-	Post-	Pre-	Post-	Post-	Post-
$N_{bt,\,tot}$ ($\times 10^{11}$/cm^2)	1.8	0.86	1.0	1.9	2.7	4.3
D_{it} ($\times 10^{12}$/cm^2 eV)	5.0–2.5	2.5–1.9	2.0–0.7	7.5–6.5	8.5–1.2	7.7–6.2
E_{it} (eV)	0.46–0.51	0.23–0.5	0.23–0.25	0.27–0.35	0.23–0.48	0.25–0.52

Without annealing, the D_{it} of the Al_2O_3 MOSCAP in this work was higher than the D_{it} of the c-plane GaN device reported in literatures for E_c–$E_{it} > 0.4$ eV characterized by the conductance method ($\sim 4 \times 10^{11}$/cm^2 eV–$\sim 6 \times 10^{11}$/cm^2 eV),[34] photo-assisted C-V method ($\sim 1.5 \times 10^{11}$/cm^2 eV),[39] and static C-V method ($\sim 2 \times 10^{11}$/cm^2 eV).[40] However, our D_{it} was comparable to the D_{it} of the c-plane GaN device reported in literatures for E_c–$E_{it} > 0.4$ eV characterized by deep level transient spectroscopy ($\sim 3 \times 10^{11}$/cm^2 eV–$\sim 8 \times 10^{11}$/cm^2 eV).[41] With annealing at 500 °C in N_2 ambient, even though our devices showed a slight reduction of D_{it} within an E_{it} in the range of 0.2 eV–0.4 eV as observed in the literature,[34] our Al_2O_3 MOSCAPs still revealed a high D_{it} compared to that of the Al_2O_3/c-plane GaN devices with annealing in N_2 ambient for an E_{it} in the range of 0.2 eV–0.5 eV below the CBM characterized by the conductance method.[34] However, our Al_2O_3 MOSCAPs showed a much lower D_{it} than Al_2O_3/c-plane GaN devices with N_2 annealing for an E_{it} in the range of 0.2 eV–0.5 eV below the CBM ($>3 \times 10^{11}$/cm^2 eV) characterized by constant capacitance deep level transient and optical spectroscopy reported by Long *et al.*[41] Compared to reported D_{it} at the Al_2O_3/m-plane GaN interface ($\sim 1.5 \times 10^{12}$/cm^2 eV for 0.2 eV–0.5 eV below the CBM[18,42]), our post-annealed device showed a similar D_{it}. The effect of annealing on Al_2O_3/non-polar GaN is similar to its effect on the Al_2O_3/Si device.[43] In our experiment, the m-plane GaN devices exhibited similar interface properties compared to c-plane GaN devices.

For the HfO_2 MOSCAP, our results were slightly better than the reported HfO_2/c-plane GaN device[44,45] even with the annealing process. After annealing, at positive bias, the leakage current and conductance increased significantly. The degraded insulting properties of oxide can be partially caused by the oxygen vacancies in the oxide.[34] Additionally, we cannot rule out the impacts of Ga native oxide regrowth at the interface and the metal dangling bonds close to the conduction band on the increase in interface states. Contrary to our observation, a reduction of D_{it} was observed at the sputtered HfO_2/c-plane GaN interface[46] and HfO_2/Si with the interfacial layer[47] after N_2 annealing. The degree of reduction depends on the annealing atmosphere and temperature. Although the vacuum annealing improved the dielectric constant (~25), it appeared that the annealing process also introduced interface traps. On a-plane GaN, in terms of D_{it}, the HfO_2 device had a slightly lower value than Al_2O_3, but the difference was insignificant. However, this difference was prone to be opposite on m-plane GaN. In fact, due to the ignored resistance during the calculation of the conductance peak (G_p/ω), the resultant D_{it} could be overestimated or underestimated. It also has been demonstrated that the annealing condition has significant influence on the interface properties in terms of D_{it}. In order to optimize the interface, an appropriate condition should be used.

IV. SUMMARY

In summary, we characterized the interface properties of ALD-dielectrics/non-polar GaN. The MOSCAPs that were fabricated on a-plane and m-plane GaN substrates with Al_2O_3 or HfO_2 as a dielectric layer were used for the electrical characterization. The impact of annealing on the density of border traps and the density of interface traps was investigated. The density of interface traps was extracted by the ac conductance method. Prior to annealing, the density of interface traps was in the magnitude of 10^{12}, and it was one order higher than the lowest reported D_{it}. Although the annealing process brought down the D_{it} of Al_2O_3 devices as expected in literatures, D_{it} was still higher than the best value. Further optimization on the process, including but not limited to the optimization of annealing conditions and the reduction of the series resistance, may be required to reduce D_{it}. By reducing leakage current, an accurate C_{ox} can be obtained and the interface traps close to the conduction band can be accessed. Temperature dependent measurements can be conducted in order to extract D_{it} located close to mid-gap.

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