1.85 kV Breakdown Voltage in Lateral Field-Plated Ga_2O_3 MOSFETs

Ke Zeng, Abhishek Vaidya, and Uttam Singisetti, *Senior Member, IEEE*

***Abstract*— A 400-nm thick composite field plate oxide, with a combination of atomic layer deposited and plasma enhanced chemical vapor deposited SiO_2 layers, is used to enhance the breakdown voltage of spin-on-glass source/drain doped lateral Ga_2O_3 MOSFET. Three terminal breakdown voltage measured in Fluorinert ambient reaches 1850 V for a L_{gd} = 20 μm device. This is the first report of lateral Ga_2O_3 MOSFET with more than 1.8 kV breakdown voltage. For a device with L_{gd} = 1.8 μm, the average electric field strength is calculated to be 2.2 ± 0.2 MV/cm while the field simulation of the device shows a peak field of 3.4 MV/cm.**

***Index Terms*— Field plate, Fluorinert, spin-on-glass, gallium oxide, SOG doping, power MOSFET, air breakdown.**

I. Introduction

β-GALLIUM oxide (Ga_2O_3) has become an increasingly attractive semiconductor for next generation power electronics applications due to its high Baliga's Figure of Merit (BFoM) [1], and also due to the mature bulk crystal growth technologies [2]–[3]. Recently, high current density transistors based on delta doping [4] and nano-membrane platform [5] are demonstrated showing its low-power loss potential and for RF applications [6]. High breakdown voltage/strength MOSFETs and diodes are also reported [7]–[13]. In particular, a record average field strength of 3.8 MV/cm is measured in a lateral MOSFET [8] and the peak field strength has reached up to 5.1 MV/cm in vertical Schottky barrier diodes [9], [12]. Both data has already surpassed the theoretical limits of bulk GaN and SiC, but still far from the empirical predicted 8 MV/cm critical electric field in Ga_2O_3 [1]. To date, the highest experimentally reported breakdown voltage (V_{BR}) in lateral MOSFET is 750V with field plate [10]. In this letter, we report an improved field plate design with composite dielectrics where a high quality ALD deposited film is used in the high field region. These devices show V_{BR} beyond 1.8 kV, which demonstrates big improvements upon the previous reports, marking an important step towards high performance Ga_2O_3 power MOSFET.

Manuscript received July 11, 2018; revised July 19, 2018; accepted July 19, 2018. Date of publication July 23, 2018; date of current version August 23, 2018. This work was supported in part by NSF monitored by Dr. D. Pavlidis under Grant ECCS 1607833 and in part by the UB ReNEW and SUNY MAM programs. The review of this letter was arranged by Editor G. H. Jessen. *(Corresponding author: Uttam Singisetti.)*

The authors are with the Electrical Engineering Department, University at Buffalo, Buffalo, NY 14260 USA (e-mail: kzeng2@buffalo.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2018.2859049

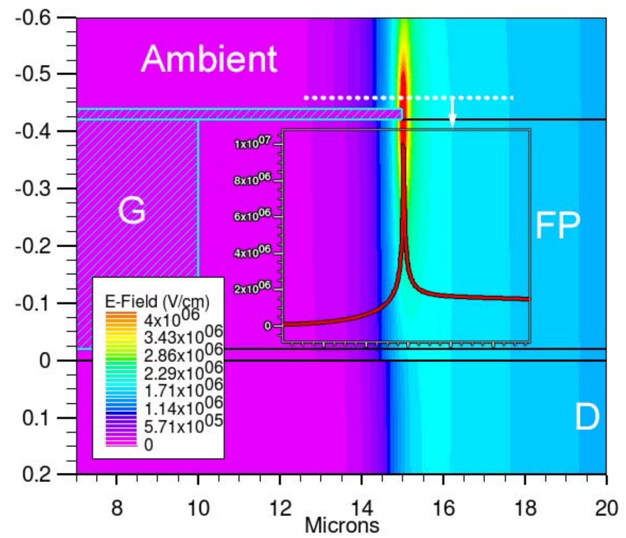

Fig. 1. Off-state TCAD electric field simulation of designed field-plated Ga_2O_3 MOSFET under 1.8kV drain bias. The peak electric field at the edge of gate electrode is present both in the oxide and in the ambient, and the field strength is almost mirror symmetrical. Overlay plot shows the cross-section field. strength in the ambient close to the gate electrode edge.

To achieve a high V_{BR} in Ga_2O_3 MOSFET, it is important to not only reduce the electric field in the Ga_2O_3 channel, but also make sure the peak field that is transferred to other locations does not create parasitic breakdown first. In a device, the catastrophic breakdown would not be determined by high quality Ga_2O_3 channel, which might be its strongest parts; it is more likely to be determined by weaker parasitic paths such as field oxide or air. Fig. 1 shows the off state ($V_g = -30$V) electric field simulation of field-plated Ga_2O_3 MOSFET under a 1.8kV drain bias using SILVACO ATLAS [14]. The dielectric constants used here are 10 for Ga_2O_3 and 3.9 for SiO_2 respectively [1]. And the field-plate oxide is modeled as single thick SiO_2 layer. No breakdown parameters (ionization coefficients) were included in material models, thus breakdown characteristics is not simulated in the device and only electric field distribution is provided. It is seen that the peak channel field (~1.6 MV/cm) is reduced compared to non-field plate device (not shown). The peak field is transferred into the

0741-3106 © 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

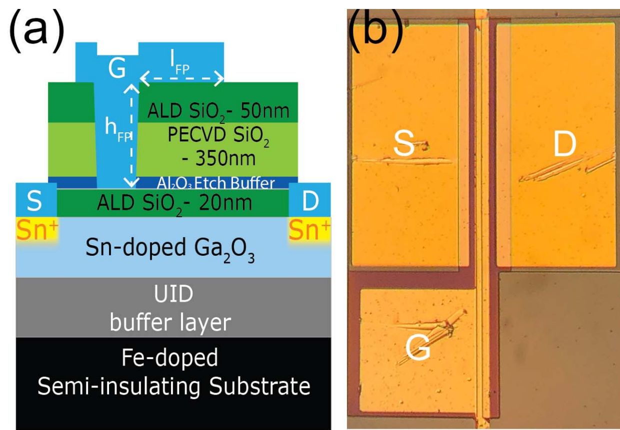

Fig. 2. (a) Cross-section view and (b) optical image of the fabricated field-plated Ga_2O_3 MOSFET with SOG S/D doping.

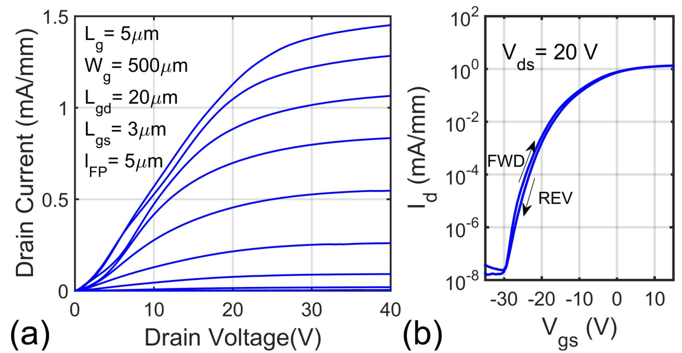

Fig. 3. (a) Output current-voltage characteristic(−20V to 12V with 4V step) and (b) transfer characteristic of fabricated field plated MOSFET with Spin-on-Glass S/D doping.

field-plate oxide with high concentration near the field plate electrode edge. However, the critical field strength of the top layer of field plate oxide is usually unclear, and property of amorphous SiO_2 varies significantly with respect to the deposition process [15]–[17]. In addition, the same peak field (∼10 MV/cm) is also present in the ambient air, which will breakdown prematurely. Air only has a dielectric strength of 30kV/cm, 266 times lower than Ga_2O_3 and 333 times lower than SiO_2 [18].

In order to eliminate the extrinsic breakdown outside the channel, a composite field-plate with denser high quality ALD SiO_2 at the top close to gate edge and a thick PECVD SiO_2 layer in the bottom is used, as shown in Fig. 2(a). The field plate extension (l_{FP}) was also optimized to reduce the peak field, with optimal length around halfway between gate and drain. If the breakdown happens inside field plate oxide, this design should give more V_{BR}. To prevent air breakdown, more passivation can be done, but in this letter, we used a dielectric liquid, Fluorinert (FC-770), [19]–[22] to replace air. It has approximately 4 times higher dielectric strength compared to air. Previously GaN [19]–[21] and SiC [22] devices used Fluorinert FC-77 liquid, to significantly improve V_{BR} compared to measurement in air owing to the higher dielectric breakdown strength of Fluorinert. Particularly, [19] and [20] have identified air breakdown as the pre-mature breakdown mechanism that clamped V_{BR} within 300- 400V range.

II. Fabrication

An MBE grown 200 nm 2×10^{17} cm^{-3}Sn-doped epitaxial layer and 200 nm of UID buffer on Fe doped semi-insulating (010) Ga_2O_3 substrate is used for device fabrication. The selective SOG doping of source/drain (S/D) is carried out as described in [7]. Ti/Au S/D contacts is then deposited in the doped region, followed by a 470°C ohmic annealing. A total of 420 nm of composite ALD/PECVD/ALD oxide layer is deposited on the sample (Fig. 2(a)). Both the top 50 nm field plate oxide and 20 nm gate dielectric SiO_2 are deposited by plasma enhanced ALD at 300 °C under 10 mT pressure, with Tris(dimethylamino)silane (3DMAS) precursor and O_2 plasma. The remaining 350 nm of SiO_2 field plate oxide is deposited by PECVD at 250 °C and 900 mT using SiH_4 and N_2O gases, while thin Al_2O_3 etch stop is deposited by thermal ALD at 300 °C using Tri-methyl Aluminum (TMA) and H_2O. A highly selective CF_4 based reactive ion etch (RIE) is then used to form the gate trench in the field plate oxide, where extremely low pressure and high ICP power is tuned to ensure a synergic etch for smooth bottom [23], a high selectivity over Al_2O_3 [24] and to form a nearly vertical sidewall profile. The Al_2O_3 layer is wet etched in photo-resist developer. This etch is followed by another 450°C 1 minute RTA to densify the stack. At last, 550nm of Ti/Al/Ni/Au contact is realigned to the trench, forming the field plate structure as shown in Fig. 2(a). Devices are finally isolated by a BCl_3/Ar RIE, which created a ∼220nm recess surrounding active region. Fig. 2(b) shows an optical image of fabricated device.

III. Results and Discussion

DC I-V characteristics are measure with HP 4155B semiconductor parameter analyzer and is shown in Fig. 3. Fig. 3(b) shows 0.8 V hysteresis in the gate voltage forward and reverse sweep. The effective channel carrier density extracted from differential CV analysis is $\sim 1.5\times10^{16}/cm^3$ [25], [26]. The reduced effective carrier density compared to initial doping density is due to the out diffusion of dopant during spin-on-glass drive-in annealing [7], [27]. The unexpected large negative V_{th} is attributed to possible charge in the oxide stack introduced during RIE process and temperature variations on the sample during the SOG drive-in annealing, thus the differential CV carrier density may not correspond to the carrier density in the FET channel. Moreover, subthreshold swing analysis gives a D_{it} $\sim 2.0\times10^{13}/cm^2{\cdot}eV$. The three terminal breakdown test is performed with a custom setup combining HP 4155B and Keithley 2657A high-voltage source-meter. For device shown in Fig. 3 with $L_{gd} = 20$ μm, the first breakdown measurement is performed with sample submerged in Fluorinert FC-770 to reduce air breakdown potential. The drain is swept from 0V to 2 kV with catastrophic breakdown measured at 1850 V. This is the highest breakdown voltage measured in a lateral Ga_2O_3 MOSFET to date. After the first sweep, the sample is taken out of Fluorinert and exposed in the air. Another breakdown test is performed in air, and device

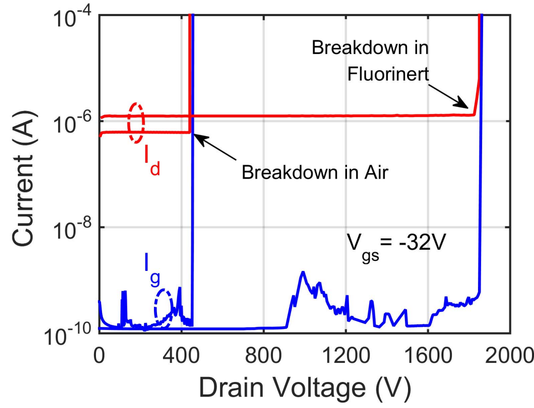

Fig. 4. Three-terminal breakdown measurement data from device under test (DUT) shown in Fig. 3. Two neighboring devices with same dimensions are measured respectively in Fluorinert and Air.

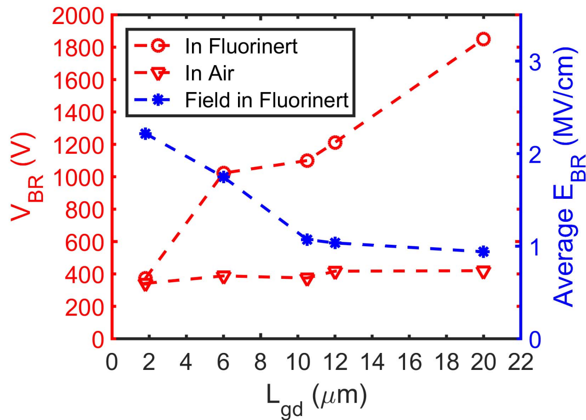

Fig. 5. Breakdown voltage V_{BR} and averaged breakdown electric field E_{BR} vs gate-drain separation L_{gd} in measured devices. The averaged breakdown field in Ga_2O_3 channel (blue asterisks, labeled "field in Flourinert") is calculated by dividing the sum of V_{BR} (measured in Fluorinert) and V_g over L_{gd}. All L_{gd} data is verified by SEM images.

had catastrophic breakdown at 440V. Both breakdown test data is shown in Fig. 4. The difference of V_{BR} with and without Fluorinert clearly shows that the breakdown without Fluorinert first happened in the air and is extrinsic to the channel.

With varying gate-drain spacing L_{gd}, multiple breakdown voltage is measured with and without Fluorinert. The average breakdown strength is also calculated by dividing net gate-drain voltage (V_{BR}-V_g) over L_{gd} [8] and is displayed in Fig. 5. As shown in Fig. 5, all devices measured a higher V_{BR} with Fluorinert, and the V_{BR} with Fluorinert is approximately 4 times higher than V_{BR} measured in the air at higher L_{gd}. Moreover, it can be seen that as L_{gd} gets smaller, E_{BR} increases rapidly. By pushing the gate and drain closer, the high field region is going to occupy more portion of the L_{gd}. For a device with $L_{gd} = 1.8\mu$m, the average electric field strength is calculated to be 2.2 ± 0.2 MV/cm and the ATLAS simulation of the device shows a peak field of 3.4 MV/cm. Moreover, due to the speculated extrinsic breakdown, the averaged field strength of 2.2 ± 0.2 MV/cm merely sets a lower bound for intrinsic Ga_2O_3 breakdown strength. Careful device engineering bearing the extrinsic breakdown in mind can push

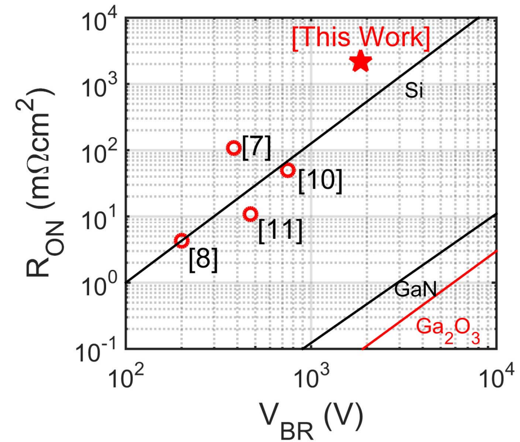

Fig. 6. Plot of R_{ON} vs. V_{BR} of DUT figure of merit against previously published lateral Ga_2O_3 MOSFETs. R_{on} in this work is calculated at V_{ds} = 10 V.

the breakdown even higher. Fig. 6 shows a comparison of R_{on} and V_{BR} in published lateral Ga_2O_3 MOSFETs.

IV. Conclusion

A composite field-plate design and Fluorinert ambient is used to effectively reduce the extrinsic breakdown potential, especially in the air. Three-terminal breakdown voltage of 1850 V is measured in a composite-field-plated Ga_2O_3 MOSFET with $L_{gd} = 20\mu$m. The breakdown voltage shows a big improvement upon previous reports, indicating the immense potential of Ga_2O_3 for high-voltage power electronics applications.

V. Acknowledgment

A portion of this work was performed in the UB shared instrumentation facility. The authors acknowledge Dr Jung-Hun Seo and Edward Swinnich for help with the breakdown measurements.

References

[1] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, p. 34001, 2016, doi: 10.1088/0268-1242/31/3/034001.

[2] H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, "Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method," *Jpn. J. Appl. Phys.*, vol. 47, no. 11R, pp. 8506–8509, Nov. 2008, doi: 10.1143/JJAP.47.8506.

[3] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, "Electrical properties of β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Appl. Phys.*, vol. 110, no. 6, p. 063720, 2011, doi: 10.1063/1.3642962.

[4] Z. Xia, C. Joishi, S. Krishnamoorthy, S. Bajaj, Y. Zhang, M. Brenner, S. Lodha, and S. Rajan, "Delta doped β-Ga_2O_3 field effect transistors with regrown ohmic contacts," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 568–571, Apr. 2018, doi: 10.1109/LED.2018.2805785.

[5] H. Zhou, K. Maize, G. Qiu, A. Shakouri, and P. D. Ye, "β-Ga_2O_3 on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect," *Appl. Phys. Lett.*, vol. 111, no. 9, p. 092102, 2017, doi: 10.1063/1.5000735.

[6] A. J. Green, K. D. Chabak, M. Baldini, N. Moser, R. Gilbert, R. C. Fitch, G. Wagner, Z. Galazka, J. Mccandless, A. Crespo, K. Leedy, and G. H. Jessen, "β-Ga_2O_3 MOSFETs for radio frequency operation," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 790–793, Jun. 2017, doi: 10.1109/LED.2017.2694805.

[7] K. Zeng, J. S. Wallace, C. Heimburger, K. Sasaki, A. Kuramata, T. Masui, J. A. Gardella, and U. Singisetti, "Ga_2O_3 MOSFETs using spin-on-glass source/drain doping technology," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 513–516, Apr. 2017, doi: 10.1109/LED.2017.2675544.

[8] A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy, and G. H. Jessen, "3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 902–905, Jul. 2016, doi: 10.1109/LED.2016.2568139.

[9] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes," *Appl. Phys. Lett.*, vol. 110, no. 10, p. 103506, 2017, doi: 10.1063/1.4977857.

[10] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 212–215, Feb. 2016, doi: 10.1109/LED.2015.2512279.

[11] K. D. Chabak, J. P. Mccandless, N. A. Moser, A. J. Green, K. Mahalingam, A. Crespo, N. Hendricks, B. M. Howe, S. E. Tetlak, K. Leedy, R. C. Fitch, D. Wakimoto, K. Sasaki, A. Kuramata, and G. H. Jessen, "Recessed-gate enhancement-mode β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 67–70, Jan. 2018, doi: 10.1109/LED.2017.2779867.

[12] X. Yan, I. S. Esqueda, J. Ma, J. Tice, H. Wang, X. Yan, I. S. Esqueda, J. Ma, J. Tice, and H. Wang, "High breakdown electric field in β-Ga_2O_3/graphene vertical barristor heterostructure," *Appl. Phys. Lett.*, vol. 112, no. 3, p. 032101, 2018, doi: 10.1063/1.5002138.

[13] J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, "High reverse breakdown voltage Schottky rectifiers without edge termination on Ga_2O_3," *Appl. Phys. Lett.*, vol. 110, no. 19, p. 192101, 2017, doi: 10.1063/1.4983203.

[14] *Atlas User's Manual*. Silvaco Int., Santa Clara, CA, USA, 2014.

[15] F. Hirose, Y. Kinoshita, S. Shibuya, Y. Narita, Y. Takahashi, H. Miya, K. Hirahara, Y. Kimura, and M. Niwano, "Atomic layer deposition of SiO_2 from Tris(dimethylamino)silane and ozone by using temperature-controlled water vapor treatment," *Thin Solid Films*, vol. 519, no. 1, pp. 270–275, 2010, doi: 10.1016/j.tsf.2010.07.107.

[16] T. Usui, C. A. Donnelly, M. Logar, R. Sinclair, J. Schoonman, and F. B. Prinz, "Approaching the limits of dielectric breakdown for SiO_2 films deposited by plasma-enhanced atomic layer deposition," *Acta Mater.*, vol. 61, no. 20, pp. 7660–7670, 2013, doi: 10.1016/j.actamat.2013.09.003.

[17] S.-J. Won, S. Suh, M. S. Huh, and H. J. Kim, "High-quality low-temperature silicon oxide by plasma-enhanced atomic layer deposition using a metal–organic silicon precursor and oxygen radical," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 857–859, Aug. 2010, doi: 10.1109/LED.2010.2049978.

[18] *Dielectric Strength of Air*. Accessed: Jul. 27, 2018. [Online]. Available: https://hypertextbook.com/facts/2000/AliceHong.shtml

[19] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 716–718, Sep. 2006, doi: 10.1109/LED.2006.881084.

[20] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 713–715, Sep. 2006, doi: 10.1109/LED.2006.881020.

[21] K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "1.7-kV and 0.55-m$\Omega\cdot$cm^2 GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.

[22] A. K. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt, "1.1 kV 4H-SiC power UMOSFETs," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 586–588, Dec. 1997, doi: 10.1109/55.644079.

[23] L. Zhang, A. Verma, H. Xing, and D. Jena, "Inductively-coupled-plasma reactive ion etching of single-crystal β-Ga_2O_3," *Jpn. J. Appl. Phys.*, vol. 56, no. 3, p. 030304, 2017, doi: 10.7567/JJAP.56.030304.

[24] S. Tegen and P. Moll, "Etch Characteristics of Al_2O_3 in ICP and MERIE plasma etchers," *J. Electrochem. Soc.*, vol. 152, no. 4, pp. G271–G276, 2005, doi: 10.1149/1.1865912.

[25] Y. Jia, K. Zeng, J. S. Wallace, J. A. Gardella, and U. Singisetti, "Spectroscopic and electrical calculation of band alignment between atomic layer deposited SiO_2 and β-Ga_2O_3 ($\bar{2}01$)," *Appl. Phys. Lett.*, vol. 106, no. 10, p. 102107, 2015, doi: 10.1063/1.4915262.

[26] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.

[27] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Anomalous Fe diffusion in Si-ion-implanted β–Ga_2O_3 and its suppression in Ga_2O_3 transistor structures through highly resistive buffer layers," *Appl. Phys. Lett.*, vol. 106, no. 3, p. 032105, 2015, doi: 10.1063/1.4906375.