Ga_2O_3 MOSFETs Using Spin-On-Glass Source/Drain Doping Technology

Ke Zeng, Joshua S. Wallace, Christopher Heimburger, Kohei Sasaki, Akito Kuramata, Takekazu Masui, Joseph A. Gardella Jr., and Uttam Singisetti, *Member, IEEE*

***Abstract*— We report the first demonstration of source/drain (S/D) doping using tin (Sn) doped spin-on-glass (SOG) on Ga_2O_3 power MOSFET. The effectiveness of SOG doping is verified by a comparative experiment on semi-insulating Ga_2O_3 substrates. A specific contact resistance of $\rho_c = 2.1 \pm 1.4 \times 10^{-5}$ Ω·cm² is obtained to the SOG doped layer. The thermal diffusion behavior of Sn in Ga_2O_3 is investigated as well. MOSFETs with SOG S/D doping is fabricated on 200-nm epitaxial Ga_2O_3 layer with an average effective doping of $2 \times 10^{17}/cm^3$. An increased peak output drain current density of 40 mA/mm is achieved due to reduced S/D resistance. The maximum transconductance (g_m) is extracted to be 1.23 mS/mm for a device with $L_g = 2\mu m$. The device also shows a large ON/OFF ratio of 10^8 and breakdown voltage of 382 V.**

***Index Terms*— Spin-on-Glass, gallium oxide, SIMS, SOG doping, power MOSFET, diffusion coefficient, ohmic contact.**

I. Introduction

GALLIUM oxide (Ga_2O_3) has been intensively studied recently due to its promising application for next generation power electronics [1]–[3]. It is reported that β-Ga_2O_3(Ga_2O_3), the most stable form of Ga_2O_3, has a high Baliga's Figure of Merit (BFoM) [4], [5]. This indicates Ga_2O_3 has a major advantage over other commonly studied wide bandgap semiconductors. Empirical calculation shows an 8 MV/cm critical electric field [4], while the most recent experimental data has reached 3.8 MV/cm [2]. This experimental data has already surpassed the theoretical limits of GaN and SiC. In addition to its excellent material property, many mature growth methods with precisely controlled doping concentration are also available today [6]–[8]. Both Ga_2O_3 field effect transistors (FETs) and Schottky diodes have been successfully demonstrated with high breakdown voltages. Depletion mode Ga_2O_3 MOSFET with high breakdown voltage is first demonstrated with Al_2O_3 gate oxide and MBE grown substrate [9]. Various enhancement mode FETs are also achieved by different techniques [1], [10], [11]. However, these devices used alloyed ohmic contacts directly to the channel which resulted in high source/drain (S/D) contact resistance and hence low drain current densities [10]. In this letter, we report a novel Spin-on-Glass (SOG) tin (Sn) doping technique for low resistance ohmic contacts to Ga_2O_3 and also show significant improvement in the device drive current.

One of the challenges with Ga_2O_3 power MOSFET is to reduce the contact resistance in order to maximize current density and reduce the conduction loss. Silicon (Si) ion-implantation has been used in the past to dope the S/D region [3], [9] and has obtained contact resistance comparable to Ti/Al based ohmic contact to n-GaN [12]. Here, we report a simple yet effective alternative –SOG doping [13]. A Sn doped SOG is spin coated on the wafer and high temperature rapid thermal annealing (RTA) is then used to drive the Sn from SOG into the substrate to dope the layer and reduce the sheet and contact resistances. The advantages of SOG doping is lower cost as an ion implanter is not needed. It also takes less process steps as a separate activation anneal is not necessary. In addition, the absence of ion-implantation damage reduces damage-induced diffusion of species [14]. Thus, SOG doping will exactly produce the exponentially decaying doping profile that can be precisely determined by interstitial diffusion model [15], [16]. SOG doping also results in highest doping density near the surface which helps in reducing the contact resistance.

II. SOG Diffusion

First, to optimize the SOG doping process, a semi-insulating Ga_2O_3 sample with iron (Fe) doping was used. The SOG used in this experiment is supplied by Desert Silicon Inc with a Sn concentration of $4 \times 10^{21}/cm^3$. The sample is first spin coated with 170 nm of SOG, it then went through a 5 minutes 1200 °C drive-in annealing in N_2 atmosphere. After annealing, the SOG layer is removed by a 10 minutes BHF treatment. The diffusion profile of the Sn in Ga_2O_3 is characterized using secondary ion mass spectroscopy (SIMS). The measured Sn doping profile is shown in Fig. 1. The blue curve is the depth profile of Sn measured by SIMS, which shows the expected Gaussian profile from diffusion from a source. The concentration of Sn drops rapidly with respect to depth, indicating a very high diffusion activation energy. The diffusion profile can be described by a single positive charged interstitial diffusion model, which is given by [17]:

$$D(T) = D_0 \exp(-\frac{D_E}{kT}) \quad (1)$$

Manuscript received February 10, 2017; revised February 23, 2017; accepted February 23, 2017. Date of publication March 1, 2017; date of current version March 22, 2017. This work was supported in part by the NSF monitored by Dr. D. Pavlidis under Grant ECCS 1607833 and in part by the UB ReNEW and SUNY MAM Programs. The review of this letter was arranged by Editor A. V. Y. Thean.

K. Zeng and U. Singisetti are with the Electrical Engineering Department, University at Buffalo, Buffalo, NY 14260 USA (e-mail: kzeng2@buffalo.edu).

J. S. Wallace, C. Heimburger, and J. A. Gardella are with the Chemistry Department, University at Buffalo, Buffalo, NY 14260 USA.

K. Sasaki, A. Kuramata, and T. Masui are with the Novel Crystal Technology, Inc., Sayama 350-1328, Japan.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2017.2675544

0741-3106 © 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

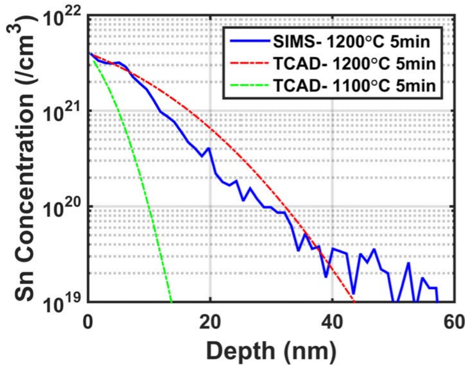

Fig. 1. Sn concentration diffused from SOG vs. depth from Ga_2O_3 interface for 1200 °C 5 min RTA sample, TCAD simulation of 1200 °C 5 min RTA sample and TCAD simulation of 1100 °C 5 min RTA sample.

where $D(T)$ (cm^2/sec) is the temperature dependent diffusion coefficient, D_0 is the pre-exponential factor, D_E is the activation energy, k is Boltzmann constant and T is the absolute temperature. The diffusion profile is simulated using Silvaco Athena simulation tool [18], with D_0 and D_E as the fitting parameter. The red dashed curve in Fig. 1 shows the simulated profile with $D_0 = 0.8$ and $D_E = 4.2$ eV. Using these parameters, the diffusion profile is simulated for an 1100 °C and 5 minute anneal. The simulated curve in Fig. 1 shows that a shallow junction can be formed for low resistance contacts, the lower temperature reduces any parasitic diffusion of dopant in the epitaxial MOSFET layers.

Next, the contact and sheet resistance of the SOG doped layer is calculated. Two identical semi-insulating Ga_2O_3 samples are used for the comparison. One Fe doped semi-insulating Ga_2O_3 sample is spin coated with 170 nm of SOG, followed by a 5 minutes 1100 °C drive-in annealing in N_2 atmosphere. This step will create a highly doped shallow junction (~ 20 nm) as predicted from simulations. After the removal of the SOG layer, a short BCl_3/Ar RIE etch was performed on the SOG doped Ga_2O_3 and another semi-insulating sample without SOG doping for ohmic contact formation [19]. Ti/Au TLM structures were then defined on both samples for resistance measurement. The samples were subsequently annealed at 450 °C for 1 minute under vacuum.

Figure. 2(a) shows the measured I-V characteristics between similar contact pads on both samples. A very low current (pA) is measured for the semi-insulating substrate. While the I-V curve for the SOG doped substrate shows substantial current with linear ohmic behavior, indicating that the diffused Sn is electrically active. Next, the contact resistance is extracted using rectangular isolated TLM structures, Fig. 2(b) shows the measured four probe resistance between two pads versus their separation. The extracted specific contact resistivity, linear contact resistance, the transfer length, and the sheet resistance are $2.1\pm1.4\times10^{-5}\Omega\cdot cm^2$, $3.4\pm0.17\ \Omega\cdot mm$, 0.48 μm and $1.0\pm0.1\times10^4\Omega/\square$ respectively. The error in the specific contact resistivity is calculated following the method in [20]. The high sheet resistance can be attributed to the ultra-shallow junction depth and lower mobility in the degenerately doped layer. Higher temperatures and longer anneal can be used to increase the junction depth and reduce the sheet resistance.

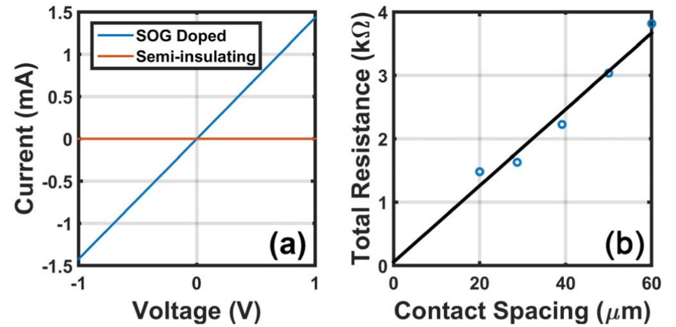

Fig. 2. (a) Comparison of the conducting current between semi-insulating layer and SOG doped layer. (b) Total resistance plotted vs. contact spacing on isolated TLM structure for SOG blanket doped sample, contact length and width are 75 μm and 150 μm respectively.

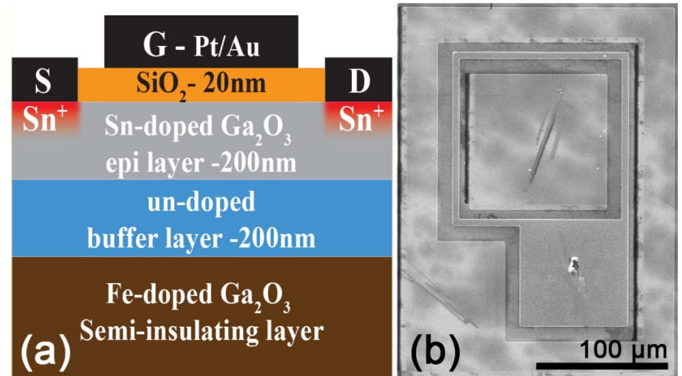

Fig. 3. (a) Cross section schematic of MOSFET with SOG doping. (b) SEM image of fabricated MOSFET with $L_g = 8\ \mu$m, drain gate spacing $L_{gd} = 10\ \mu$m.

III. SOG Doped S/D MOSFET

After confirming the SOG doping process, Ga_2O_3 MOSFET was fabricated incorporating the SOG doped source/drain. The cross-section schematic of the MOSFET is shown in Fig. 3. A 200 nm Sn-doped epitaxial layer with a doping density of $1\times10^{18}/cm^3$ was grown by ozone MBE on Fe doped semi-insulating Ga_2O_3 substrate with a 200 nm un-doped buffer layer to hinder the diffusion of Fe into doped channel layer [3], [21]. The sample is first spin coated with blanket SOG layer. In order to dope only S/D region, the SOG is patterned and etched in a CF_4/O_2 RIE process to preserve the SOG only on top of the S/D regions. Next, a 5 minutes 1100 °C drive-in annealing is carried out and Ti/Au contacts are formed as described in the previous section. A blanket layer of 20 nm SiO_2 was then deposited on the wafer by plasma enhanced atomic layer deposition (ALD) as the gate oxide [10], [22], which is followed by gate photolithography and Pt/Au metallization. The oxide covering S/D contact is then removed by an RIE etch for probing of the device. Finally, a 450 °C, 1 minute annealing is performed to improve oxide quality.

The measured MOSCAP C-V profile and the extracted electron density profile [23], [24] under the gate is shown in Fig. 4 (a) and Fig. 4(b) respectively. It is observed that the doping concentration is not uniform under the gate, and the effective channel doping is $2\times10^{17}/cm^3$. The non-uniform

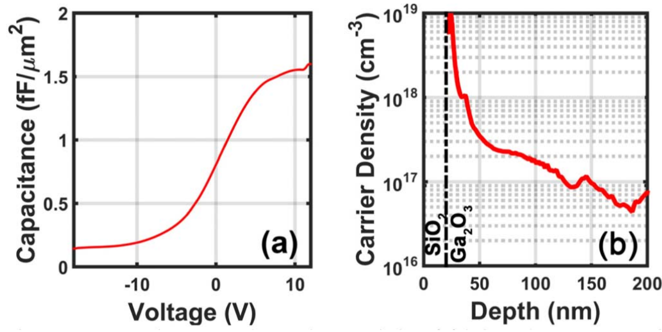

Fig. 4. (a) Capacitance- Voltage characteristic of fabricated MOSFETs with SOG doping at S/D region. (b) Carrier density profile extracted using differential capacitance method, depth starts from gate/oxide interface. Doping in the channel is decreasing with depth due to its out-diffusion towards buffer layer.

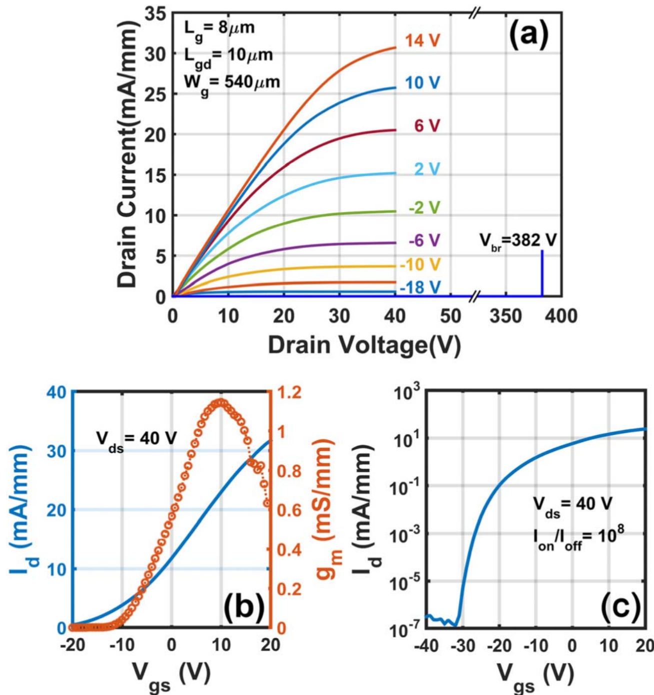

Fig. 5. (a) Output characteristics of the SOG S/D doped MOSFET with $L_g = 8$ μm, drain gate spacing $L_{gd} = 10$ μm. (b) and (c) are linear and log scale transfer characteristics of the same device measured at $V_{ds} = 40$V, ON/OFF ratio is 10^8.

doping profile is likely due to the out diffusion of dopant in the channel during drive-in annealing for SOG. Figure. 5(a) shows the output current-voltage characteristic of MOSFET with $L_g = 8\,\mu$m, maximum drain current density of 35mA/mm is obtained. The current density is increased by approximately three orders from MOSFETs with no SOG doping [10] due to the reduced contact and source access resistances. The measured current density is comparable with other reported devices with similar doping density with ion-implanted S/D regions [9]. Figures 5(b) and (c) show the transfer characteristic of the MOSFET, the peak transconductance (g_m) is extracted to be 1.15 mS/mm at $V_{gs} = 10$ V and the ON/OFF ratio is 10^8. Figure 6 shows a linear scaling of g_m on gate length (L_g), where the highest g_m obtained

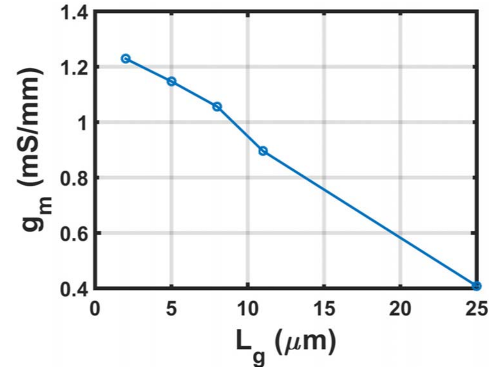

Fig. 6. Linear dependence of transconductance g_m vs. gate length L_g.

is 1.23 mS/mm when $L_g = 2\mu$m. Three terminal breakdown test is performed at a gate bias of -25V, and the measured breakdown voltage is 382 V. This value is similar to the previous reported breakdown voltage with similar device dimensions [10].

IV. Conclusion

A novel SOG doping scheme for contacts is demonstrated. Specific contact resistance measurement on the shallow junctions formed by SOG doping is measured to be $\rho_c = 2.1\pm1.4\times10^{-5}\Omega\cdot\text{cm}^2$. Ga_2O_3 MOSFET with S/D SOG doping was fabricated to confirm the effectiveness of this doping method. An improved peak current density of 40 mA/mm and peak transconductance of $g_m = 1.23$ mS/mm is achieved with this method for $L_g = 2$ μm device. The devices also show large ON/OFF ratio and maintain a high breakdown voltage even after the high temperature dopant drive in anneal. In conclusion, SOG doping provides a simple, low cost and effective way to make ohmic contact to lower doped Ga_2O_3 channel.

V. Acknowledgment

A portion of this work was performed in the UB shared instrumentation facility.

References

[1] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. Ye, "High-performance depletion/enhancement-ode β-Ga_2O_3 on insulator (GOOI) field-effect transistors with record drain currents of 600/450 mA/mm," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 103–106, Jan. 2017, doi: 10.1109/LED.2016.2635579.

[2] A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy, and G. H. Jessen, "3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 902–905, Jul. 2016, doi: 10.1109/LED.2016.2568139.

[3] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 212–215, Feb. 2016, doi: 10.1109/LED.2015.2512279.

[4] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Development of gallium oxide power devices," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 211, no. 1, pp. 21–26, Jan. 2014, doi: 10.1002/pssa.201330197.

[5] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, p. 34001, 2016, doi: 10.1088/0268-1242/31/3/034001.

[6] K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, and S. Yamakoshi, "Device-quality β-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy," *Appl. Phys. Exp.*, vol. 5, no. 3, p. 35502, Feb. 2012, doi: 10.1143/APEX.5.035502.

[7] H. Murakami, K. Nomura, K. Goto, K. Sasaki, K. Kawara, Q. T. Thieu, R. Togashi, Y. Kumagai, M. Higashiwaki, A. Kuramata, S. Yamakoshi, B. Monemar, and A. Koukitu, "Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy," *Appl. Phys. Exp.*, vol. 8, no. 1, p. 15503, 2015, doi: 10.7567/APEX.8.015503.

[8] M. Baldini, M. Albrecht, A. Fiedler, K. Irmscher, D. Klimm, R. Schewski, and G. Wagner, "Semiconducting Sn-doped β-Ga_2O_3 homoepitaxial layers grown by metal organic vapour-phase epitaxy," *J. Mater. Sci.*, vol. 51, no. 7, pp. 3650–3656, Apr. 2016, doi: 10.1007/s10853-015-9693-6.

[9] M. Higashiwaki, K. Sasaki, T. Kamimura, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, "Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics," *Appl. Phys. Lett.*, vol. 103, no. 12, p. 123511, 2013, doi: 10.1063/1.4821858.

[10] K. Zeng, K. Sasaki, A. Kuramata, T. Masui, and U. Singisetti, "Depletion and enhancement mode β-Ga_2O_3 MOSFETs with ALD SiO_2 gate and near 400 V breakdown voltage," in *Proc. 74th IEEE Device Res. Conf. (DRC)*, Jun. 2016, pp. 1–2, doi: 10.1109/DRC.2016.7548430.

[11] K. D. Chabak, N. Moser, A. J. Green, D. E. Walker, Jr., S. E. Tetlak, E. Heller, A. Crespo, R. Fitch, J. P. McCandless, K. Leedy, M. Baldini, G. Wagner, Z. Galazka, X. Li, and G. Jessen, "Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage," *Appl. Phys. Lett.*, vol. 109, no. 21, p. 213501, 2016, doi: 10.1063/1.4967931.

[12] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Si-ion implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts," *Appl. Phys. Exp.*, vol. 6, no. 8, p. 86502, 2013, doi: 10.7567/APEX.6.086502.

[13] A. Usami, M. Ando, M. Tsunekane, and T. Wada, "Shallow-junction formation on silicon by rapid thermal diffusion of impurities from a spin-on source," *IEEE Trans. Electron Devices*, vol. 3, no. 1, pp. 105–110, Jan. 1992, doi: 10.1109/16.108218.

[14] L. H. Zhang, K. S. Jones, P. H. Chi, and D. S. Simons, "Transient enhanced diffusion without {311} defects in low energy B^+-implanted silicon," *Appl. Phys. Lett.*, vol. 67, no. 14, p. 2025, 1995, doi: 10.1063/1.114775.

[15] M. E. Greiner and J. F. Gibbons, "Diffusion of silicon in gallium arsenide using rapid thermal processing: Experiment and model," *Appl. Phys. Lett.*, vol. 44, no. 8, pp. 750–752, 1984, doi: 10.1063/1.94904.

[16] C. S. Hernandes, J. W. Swart, M. A. A. Pudenzi, G. T. Kraus, Y. Shacham-Diamand, and E. P. Giannelis, "Rapid thermal diffusion of Sn from spin-on-glass into GaAs," *J. Electrochem. Soc.*, vol. 142, no. 8, pp. 2829–2832, 1995, doi: 10.1149/1.2050099.

[17] J. D. McBrayer, R. M. Swanson, and T. W. Sigmon, "Diffusion of metals in silicon dioxide," *J. Electrochem. Soc.*, vol. 133, no. 6, pp. 1242–1246, 1986, doi: 10.1149/1.2108827.

[18] *Athena User's Manual*, Silvaco Int., Santa Clara, CA, USA, 2014.

[19] T. Kamimura, K. Sasaki, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, S. Yamakoshi, and M. Higashiwaki, "Band alignment and electrical properties of Al_2O_3/β-Ga_2O_3 heterojunctions," *Appl. Phys. Lett.*, vol. 104, no. 19, p. 192104, May 2014, doi: 10.1063/1.4876920.

[20] H.-J. Ueng, D. B. Janes, and K. J. Webb, "Error analysis leading to design criteria for transmission line model characterization of ohmic contacts," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 758–766, Apr. 2001, doi: 10.1109/16.915721.

[21] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Anomalous Fe diffusion in Si-ion-implanted β–Ga_2O_3 and its suppression in Ga_2O_3 transistor structures through highly resistive buffer layers," *Appl. Phys. Lett.*, vol. 106, no. 3, p. 032105, 2015, doi: 10.1063/1.4906375.

[22] S. Won, S. Suh, M. S. Huh, and H. J. Kim, "High-quality low-temperature silicon oxide by plasma-enhanced atomic layer deposition using a metal–organic silicon precursor and oxygen radical," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 857–859, Aug. 2010, doi: 10.1109/LED.2010.2049978.

[23] Y. Jia, K. Zeng, J. S. Wallace, J. A. Gardella, and U. Singisetti, "Spectroscopic and electrical calculation of band alignment between atomic layer deposited SiO_2 and β-Ga_2O_3 $(\bar{2}01)$," *Appl. Phys. Lett.*, vol. 106, no. 10, p. 102107, 2015, doi: 10.1063/1.4915262.

[24] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.