Interface State Density in Atomic Layer Deposited $SiO_2/\beta\text{-}Ga_2O_3$ ($\bar{2}01$) MOSCAPs

Ke Zeng, Ye Jia, and Uttam Singisetti, *Member, IEEE*

***Abstract*— The interface state density (D_{it}) at the interface between β-Ga_2O_3 ($\bar{2}01$) and atomic layer deposited (ALD) SiO_2 dielectric is extracted using Terman method and conductance method. The effect of the different surface treatments on the extracted D_{it} was also studied. It is observed that the extracted D_{it} of 6×10^{11} $cm^{-2}eV^{-1}$ for the sample with no surface treatment is lower than hydrofluoric and hydrochloric acid treated samples. Low D_{it} sample shows narrow peak in the conductance method, suggesting a smooth interface. The extracted low D_{it} makes ALD SiO_2 an attractive candidate for future Ga_2O_3 power devices.**

***Index Terms*— Gallium oxide, ALD silicon dioxide, interface state, conductance method, Terman method.**

I. Introduction

WIDE bandgap semiconductor β-Ga_2O_3 (Ga_2O_3) has recently attracted a lot of attention due to its potential for next generation power electronics. Ga_2O_3 has been reported to have high Baliga's Figure of Merit (BFoM), a figure of merit for power devices, next to diamond among all the commonly studied wide bandgap semiconductor materials [1]. Besides excellent material properties, a mature growth technology for large area substrates is another practical advantage for cost effectiveness [2], [3]. MOSFETs and Schottky diodes based on β-Ga_2O_3 with high breakdown voltages have been successfully demonstrated [4], [5]. In these devices, atomic layer deposited Al_2O_3 has been used as the gate barrier due to its high dielectric constant and large conduction band-offset. However, it was recently reported that SiO_2/Ga_2O_3 interface has a much bigger conduction band offset than that of Al_2O_3/Ga_2O_3 [6]. Large conduction bandoffset can reduce gate leakage and therefore, can potentially improve the device performance. Besides bandoffset, the electrical properties of the interface will also impact device performance [7]. In particular, the interface state density (D_{it}) not only affects the gate modulation of the channel creating threshold voltage (V_{th}) instability, but also plays a role in the variation of channel mobility. In order to reach full potential of SiO_2/Ga_2O_3 based power devices, the interface state density needs to be characterized. In this letter, interface state densities of SiO_2/Ga_2O_3 metal oxide semiconductor (MOS) structure with different surface treatment are investigated by two methods: Terman method and conductance method. The implication of the data and the limitations of methods are also discussed.

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The authors are with the Electrical Engineering Department, University at Buffalo, The State University of New York, Buffalo, NY 14260 USA (e-mail: uttamsin@buffalo.edu).

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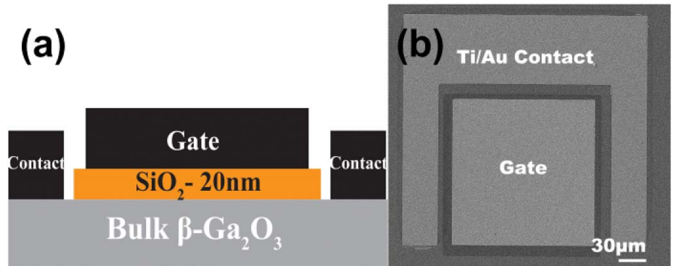

Fig. 1. (a) Cross section schematic of MOSCAP structure. (b) SEM image of fabricated 100 μm × 100 μm MOSCAP.

II. Experiments

MOS capacitance (MOSCAP) structures, shown in Fig. 1(a), with different sizes were used here for interface state density characterization. The interface state density at semiconductor/dielectric interfaces have been reported to decrease with various surface treatments [8]. To study the effect of wet chemical surface treatment, samples with hydrofluoric (HF) and hydrochloric (HCl) acid surface treatment have been analyzed together with samples with no treatment. The Ga_2O_3 substrates studied here were grown by Tamura Corporation with a Sn doping density of $9\times10^{18}/cm^3$. Three bare β-Ga_2O_3 samples were cleaved from this substrate and the samples were cleaned in standard solvents and rinsed in deionized (DI) water. One was then dipped in HF for 1 minutes, another dipped in HCl for 1 minutes and both were subsequently rinsed for 1 minute in deionized (DI) water. The treatment of HF and HCl did not create any visible chemical reaction and no measurable etching was observed in atomic force microscopy (AFM) analysis. The measured root mean square surface roughness for all the samples was $\sim$ 0.2-0.3 nm. A 20 nm layer of SiO_2 was then deposited by atomic layer deposition (ALD) for all three samples at the same time. The thickness of the deposited SiO_2 film was verified on a Si monitor wafer by spectroscopic ellipsometer. For MOSCAP fabrication, the Ti/Au gate electrodes were first defined by standard photolithography and lift-off procedure. Then, silicon dioxide layer was etched away by CF_4/O_2 based reactive ion etching (RIE) at contact regions. Before deposition of Ti/Au ohmic contacts, a BCl_3/Ar etch was performed. Then Ti/Au contact metals were deposited, followed by annealing at 470 °C for 1 minutes to make

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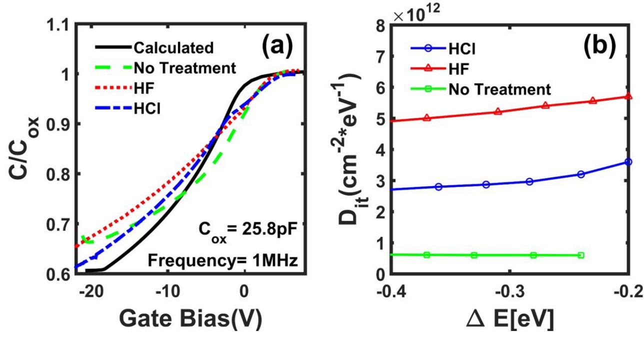

Fig. 2. (a) Comparison of calculated ideal C-V and measured C-V curves of samples with different surface treatment. (b) Interface trap density D_{it} versus energy level ΔE derived from C-V measurement using Terman method for three samples. Size of the MOSCAP is 100 μm $\times$ 150 μm.

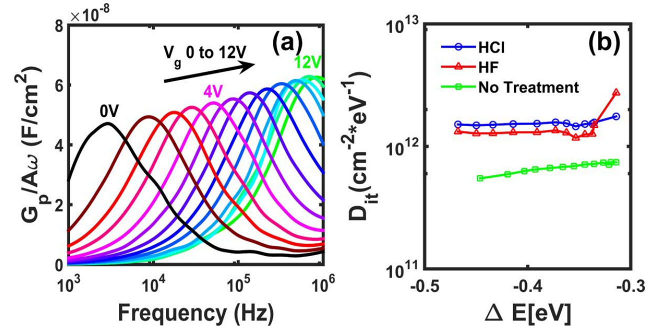

Fig. 3. (a) Normalized equivalent conductance spectrum at various gate bias derived from measured conductance data for the sample with no treatment. (b) Interface trap density D_{it} versus energy level ΔE derived from the peak value of normalized conductance spectrum. Conductance was measured at 300K. Size of the MOSCAP is 100 μm $\times$ 150 μm.

the contacts ohmic [4]. Scanning electron microscope (SEM) image of one fabricated device is shown in Fig. 1(b).

III. Results and Discussion

The interface state density was first extracted using Terman method [9]. In this method, a measured high frequency (hf) C-V curve is compared with an ideal calculated C-V curve to generate interface trap density distribution over bandgap. The ideal C-V curve was calculated numerically using MATLAB [11] from the exact solution of the electrostatics model of the MOSCAP with a doping density of 9×10^{18} cm^{-3}. Deep depletion was include in the calculation [12]. The band alignment parameters reported in [6] was used in the calculations. The hf C-V was measured at 1 MHz frequency assuming the interface traps do not respond to the hf ac excitation, but will follow the slowly varying dc bias. Fig. 2(a) shows the calculated C-V curve and measured 1 MHz C-V curves from 100 μm $\times$ 150 μm devices. The flat band voltage (V_{FB}) evaluated from the C-V curve is $\sim$5.1 V which gives an oxide trapped sheet charge density of 5.5×10^{12} cm^{-2}. The horizontal stretch out of the measured curves in the figure is an indication of interface state density response to the slowly varying gate bias. It can be seen that the stretch out of the sample with no treatment is lower than HF and HCl treated samples, indicating a lower D_{it}. The interface trap density can be determined from the stretch out of the measured curves by [9]:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_g}{d\varphi_s} - 1\right) - \frac{C_s}{q} = \frac{C_{ox}}{q^2}\frac{d\Delta V_g}{d\varphi_s}, \quad (1)$$

where $\Delta V_g = V_g$ (measured)- V_g (ideal), and φ_s is surface potential and C_s is semiconductor capacitance. In the simulated ideal C-V curve, each gate bias V_g correspond to a surface potential φ_s. Therefore, calculated D_{it} at each φ_s point can generate a plot of D_{it} vs. ΔE. However, the energy range where the Terman method gives accurate D_{it} is significantly limited by the hf ac frequency and dc sweep rate [14]. With ac frequency of 1 MHz and a dc sweep rate of $\sim$3 V/s, only traps between 0.2 and 0.4 eV below conduction band can be accurately measured and they are shown in Fig. 2(b).

Fig. 2(b) also shows that HCl and HF treated MOSCAPs have comparable D_{it}, while sample with no treatment shows lower D_{it}. The D_{it} extracted from Terman method for sample with no treatment, HF treated and HCl treated samples are 6.5×10^{11} cm^{-2}eV^{-1}, 4.9×10^{12} cm^{-2}eV^{-1} and 2.7×10^{12} cm^{-2}eV^{-1} respectively, at 0.4 eV below conduction band. Terman method has been most critiqued for the uncertainty of generated ideal C-V curve and also due to the C-V curve stretch out by the border traps [9]. Also, in the calculation of ideal C-V curve, the slope changes significantly with doping density N_D which adds some uncertainty to the result. However, as described in section II, all the three samples reported here were fabricated on the same substrate with a constant N_D, Terman method gives good information about the relative difference of D_{it} on the three samples.

The D_{it} was also extracted using conductance method. Compared to Terman method, conductance method is much slower and requires higher precision of measurement but has been shown to be very accurate for determining D_{it} in semiconductor interfaces [10], [13]. However, the D_{it} is characterized only over a narrow range in the bandgap due to the limitations of measurement temperature and frequency. At various gate biases, the ac conductance (G_m) and the capacitance (C_m) of the MOSCAPs were measured using Agilent 42941A impedance probe kit and Agilent 4294A from 1 kHz to 1 MHz. From the measured ac conductance, the normalized equivalent parallel conductance is calculated by [10], [13]:

$$\frac{\langle G_P \rangle}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (2)$$

where C_{ox} is the oxide capacitance measured in accumulation, G_m and C_m were measured conductance and capacitance respectively, and ω is the angular frequency of measurement. The extracted equivalent conductance (G_p) versus measurement frequency for the sample with no treatment is shown in Fig. 3(a). The sharp and narrow peaks correspond to interface states' response and the modulation of the peak position with gate bias is also as expected [14]. In addition, the peak is very narrow ($G_{p,peak}$/5 spans only one order in bandwidth) compared to SiC/dielectric interfaces [14], which suggests a small time constant dispersion [13]. This is one of the attributes of a good interface. From the conductance peak,

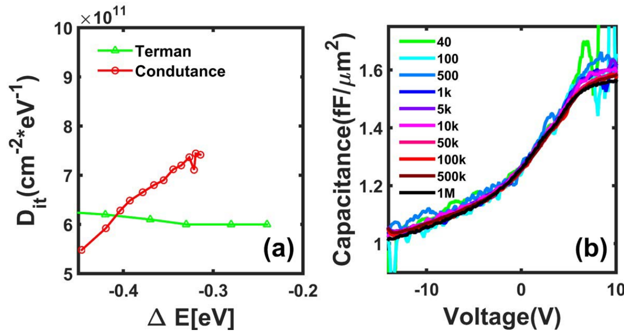

Fig. 4. (a) Combined D_{it} versus ΔE plot for sample with no treatment. (b) Frequency dependent C-V curve for sample with no treatment 300K. It shows very small frequency dispersion. Size of the MOSCAP is 150 μm × 225 μm. DC sweep rate is 0.05 V/s.

the interface trap density can be calculated using [10]:

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{peak}, \tag{3}$$

where A is area of device. The location of the D_{it} in the bandgap (ΔE) can be calculated by Shockley–Read–Hall statistics of capture and emission rates [10],

$$\tau = \frac{\exp\left(\frac{\Delta E}{kT}\right)}{\sigma v_t N}, \tag{4}$$

where $\tau = 2\pi/\omega$, σ is the capture cross section of the trap and the value 1×10^{-15} cm^2 is used [16], v_t is average thermal velocity of majority carriers, N is the effective density of states of the majority carrier band, k is the Boltzmann constant and T is the temperature. Fig. 3(b) shows the calculated D_{it} vs. ΔE obtained from the conductance method for all the samples. It is again seen that the extracted D_{it} is lower for the sample with no treatment as compared to HF and HCl treated samples, which is consistent with Terman method result in Fig. 2(b).

Note in Fig. 3(b), the characterized trap energy range is very close to conduction band because the samples were measured at room temperature. To put the two methods into perspective, Fig. 4(a) shows a combined plot of results from conductance method and Terman method for sample with no treatment. It can be seen that the results are very similar at conduction band edge.

Fig. 4(b) shows the frequency dispersion of the C-V curves for sample with no treatment, a very small dispersion of about 1% is observed over large range of frequencies (40 Hz to 1 MHz) in the depletion region ($V_g < 5$ V), which is also an indication of low D_{it} interface. Using the Hi-Lo method proposed by Castagné and Vapaille [17], the peak D_{it} is extracted from ΔC of 1 MHz and 40 Hz CV curve at $V_g \approx 5$ V to be 2.6×10^{10} cm^{-2}eV^{-1} at ~0.2 eV below conduction band using:

$$D_{it} = \left(\frac{C_{ox}C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox}-C_{HF}}\right)/qA, \tag{5}$$

where C_{ox} is the capacitance at accumulation, C_{LF} and C_{HF} are the measured low and high frequency CV curves. This value is lower than the value calculated from Terman and conductance method because 40 Hz is not low enough and some interface states still cannot respond to the ac signal. The low frequency C-V in accumulation ($V_g > 5$ V) shows noise caused by the gate leakage in the 20 nm thick oxide layer.

It is noted that the D_{it} is determined close to the conduction band, the methods used here do not throw any insight on D_{it} in deep levels. Using temperature dependent C-V can further increase the range of D_{it}, but D_{it} below midgap can still not be probed due to the absence of p-type doping in Ga_2O_3. However, in a MOSFET operation, D_{it} within the range of the Fermi-level movement will influence device operation.

IV. Conclusion

In summary, we evaluated the Ga_2O_3-SiO_2 interface state density by MOSCAP C-V and G-V measurements. Terman method and conductance method were used to extract the D_{it}. From both methods, the interface trap density close to the conduction band is low (~6×10^{11} cm^{-2}eV^{-1}) for the sample with no treatment. However, the D_{it} is increased for HF and HCl treated samples to 2×10^{12} cm^{-2}eV^{-1}. The low D_{it} in the untreated samples will have minimal effect on the device performance. Terman method, conductance method and low frequency dispersion indicate a good interface between Ga_2O_3 and SiO_2. Although the treatment of HCl and HF did not improve the D_{it}, it provided a useful reference for future experiments. More sophisticated interface treatment, like RCA clean [16], may be required to further reduce D_{it}.

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