Enhancement-Mode N-Polar GaN MOS-HFET With 5-nm GaN Channel, 510-mS/mm g_m, and 0.66-$\Omega \cdot$ mm $R_{\rm on}$

Uttam Singisetti, Man Hoi Wong, James S. Speck, and Umesh K. Mishra

***Abstract*—We report enhanced dc and small-signal RF performance of enhancement-mode (E-mode) metal–oxide–semiconductor heterojunction field-effect transistors (MOS-HFETs) in N-polar GaN technology with an ultrathin 5-nm GaN channel and graded AlGaN back-barrier structure with a record on-resistance ($R_{\rm on}$) of 0.66 $\Omega \cdot$ mm. The device has a maximum drain current (I_d) of 1.15 A/mm, a peak transconductance (g_m) of 510 mS/mm, and a peak current-gain cutoff frequency (f_t) of 122 GHz, with a positive threshold voltage ($V_{\rm th}$) of 1.6 V. The device shows improved saturation and pinchoff characteristics compared to the previously reported N-polar E-mode HFETs with a maximum $I_{\rm on}/I_{\rm off}$ ratio of 2.2×10^5.**

***Index Terms*—ALD Al_2O_3, AlGaN/GaN HEMT, enhancement mode, GaN high-k dielectric, GaN MOS-HFET, lowest R_{on}, N-polar GaN HEMT, self-aligned.**

I. Introduction

USING novel technologies such as InAlN barrier for high aspect ratio, AlGaN back barrier for increased carrier confinement, regrowth of source/drain regions to reduce contact resistances, and the reduction of source–drain distance to reduce parasitic resistances, the bandwidth of GaN field-effect transistors (FETs) has recently been extended to a current-gain cutoff frequency (f_t) of 260 GHz and a power-gain cutoff frequency ($f_{\rm max}$) of 400 GHz [1]–[4]. N-polar GaN FETs are being explored because of their potential advantage in scaling due to the confinement provided by the wide bandgap back barrier [5], [6]. Enhancement-mode (E-mode) N-polar GaN FETs with a GaN quantum well channel thickness of 8 nm, which employed self-aligned source/drain regrowth and SiN_x gate dielectrics by high-temperature chemical vapor deposition, have recently been demonstrated that show a peak f_t of 120 GHz at a gate length (L_g) of 70 nm [7]. Despite good RF performance, these devices show poor saturation and pinchoff characteristics because of the drain modulation of the channel electrostatics by the trap at the negative-polarization (AlN/GaN-buffer) interface [8], as well as the low aspect ratio. In addition, the device shows high source resistance because of surface depletion, and lower mobility (350 $\rm cm^2/V \cdot s$) in the access regions due to the close proximity of the 2-D electron gas (2DEG) to the surface in the 8-nm GaN channel device as compared to the 20-nm GaN channel device reported in [9]. Further scaling of the gate length to sub-50-nm dimensions would require vertical scaling of the GaN channel thickness to 5 nm and the incorporation of a high-k gate dielectric to achieve a high aspect ratio to reduce short-channel effects, as well as to maintain a positive threshold voltage ($V_{\rm th}$). The close proximity of the surface to the 2DEG in the ultrascaled 5-nm GaN channel amplifies both the surface depletion and the surface scattering of the 2DEG which increases the parasitic access resistances. This problem becomes critical in the E-mode devices because of the lower modulation doping compared to depletion mode (D-mode) devices to ensure positive $V_{\rm th}$.

Using a graded AlGaN back-barrier design to reduce the drain modulation caused by the negative-polarization interface and to improve electron mobility in ultrathin channels, as well as optimizing the regrowth condition to get complete InN coverage to reduce the surface depletion, we report in this letter an E-mode N-polar GaN metal–oxide–semiconductor heterojunction FET (MOS-HFET) with an ultrathin 5-nm GaN channel and an Al_2O_3 gate dielectric by atomic layer deposition (ALD). These devices show greatly improved peak drive current (I_d), peak transconductance (g_m), and peak $I_{\rm on}/I_{\rm off}$ ratio of 1.15 A/mm, 510 mS/mm, and 2.2×10^5, respectively. Devices with an L_g of 115 nm show a peak f_t of 122 GHz and an associated $f_t - L_g$ product of 14 GHz $\cdot \mu$m. The on-resistance ($R_{\rm on}$) of 0.66 $\Omega \cdot$ mm is the lowest reported for E-mode GaN FETs [3], [10], [11].

II. Device Structure and Fabrication

The E-mode N-polar self-aligned device structure and fabrication process are described in detail in [7] and [9]. Fig. 1 shows the band diagrams under the gate and the sidewall access regions. The device structure consists of a 5-nm GaN channel with a 2.5-nm AlN cap layer, a 2-nm AlN back barrier, a 5-nm unintentionally doped (UID) $Al_{0.40}Ga_{0.60}N$ setback layer, a 30-nm graded AlGaN modulation doping layer ($[Si] = 6 \times 10^{18}$ $\rm cm^{-3}$), and a GaN buffer grown on a C-face SiC substrate by plasma-assisted molecular beam epitaxy (PA-MBE). E-mode operation is achieved due to the depletion

Manuscript received September 18, 2011; accepted September 28, 2011. Date of publication November 7, 2011; date of current version December 23, 2011. This work was supported by the Defense Advanced Research Projects Agency NeXT Program. The review of this letter was arranged by Editor G. Meneghesso.

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Digital Object Identifier 10.1109/LED.2011.2170656

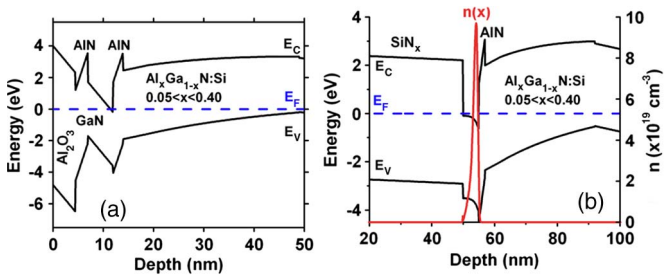

Fig. 1. (a) Simulated band diagram under the gate. The thickness of the grade is 30 nm, and the Si modulation doping in the grade is 6×10^{18} cm^{-3}. There is 5 nm of UID $Al_{0.40}Ga_{0.60}N$ between the modulation doped layer and the AlN back barrier. (b) Simulated band diagram under the SiN_x sidewall access region.

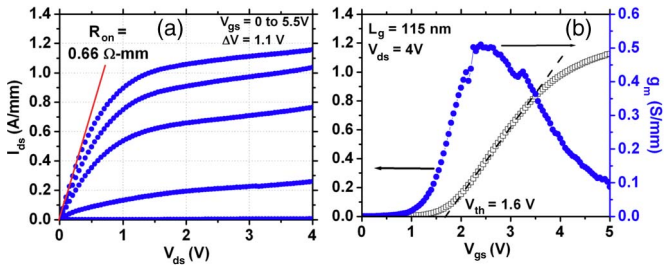

Fig. 2. DC (a) output and (b) input characteristics of the 115-nm gate length device. The foot dimension of the W-gate was verified by SEM.

of the 2DEG by the top AlN layer, surface depletion, and depletion from trapped charges in the gate dielectric [Fig. 1(a)]. Unlike the devices reported in [7] and [9], a graded AlGaN back barrier is used to reduce the output conductance caused by the negative-polarization interface below the channel [8]. After the MBE growth of the device, 4.5 nm of Al_2O_3 was deposited in an ALD chamber with trimethyl aluminum and H_2O precursors [12]. W/Cr/SiN_x gates were then fabricated, following the process in [7] and [9]. After the W/Cr/SiN_x-gate formation, the Al_2O_3 gate dielectric was wet etched in buffered HF for 15 s, which was followed by a selective wet etch of the AlN layer, stopping on the 5-nm GaN channel [7], [9]. Next, 30-nm SiN_x sidewalls were deposited by plasma-enhanced chemical vapor deposition (PECVD), and graded n^{++} InGaN/InN source/drain regions were formed by PA-MBE regrowth [13]. Removal of the AlN cap layer and deposition of the PECVD SiN_x recover a simulated 2DEG charge density of 1.8×10^{13} cm^{-2} under the sidewall regions [Fig. 1(b)]. Finally, nonalloyed Ti/Au source/drain ohmic contacts with a source–drain contact spacing of 0.5 μm were defined, and the devices were mesa isolated in a Cl_2 base RIE etch.

III. Results and Discussion

Fig. 2 shows the dc output and input characteristics of a 115-nm gate length FET with a maximum I_d of 1.15 A/mm at $V_{gs} = 5.5$ V and $V_{ds} = 4.0$ V, and a peak g_m of 510 mS/mm at $V_{gs} = 2.5$ V and $V_{ds} = 4.0$ V. A positive threshold voltage of 1.6 V is extracted from the linear extrapolation of the I_d–V_g plot. The R_{on} of the device is 0.66 Ω · mm. This is the lowest reported R_{on} value for E-mode GaN FETs on any polarity. The low R_{on} is achieved by increasing the Si doping in the

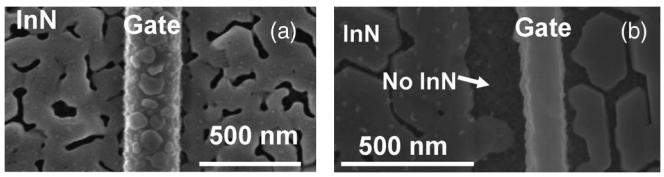

Fig. 3. SEM images of InN regrowth coverage near the gate for (a) the optimized InN regrowth condition for devices reported in this letter and (b) the unoptimized InN regrowth condition in the previously reported devices [7], [11], showing the difference in InN coverage near the gate.

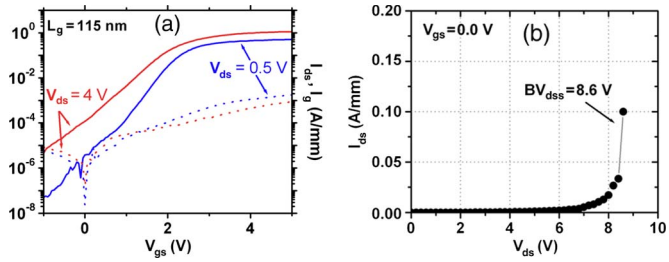

Fig. 4. (a) Plot of log I_{ds} versus V_{gs} and log I_g versus V_{gs} for drain bias values of 0.5 and 4.0 V, respectively. (b) Breakdown characteristics of the device at $V_{gs} = 0$ V.

InGaN regrowth to $> 1 \times 10^{20}$ cm^{-3} and also by optimizing the regrowth condition which improved the InN coverage near the gate [Fig. 3(a)] compared to the previously reported E-mode devices [Fig. 3(b)] in [7] and [9]. Complete coverage of InN is achieved by using a lower InN regrowth temperature of 450 °C to reduce decomposition and increasing the InN growth time. The surface Fermi-level pinning of the InN is within the conduction band and thus reduces the depletion of electrons in the device access regions [13]. A sheet resistance of 490 Ω/□ is measured for the sidewall regions on a process monitor sample with a 2DEG density (n_s) of 1.7×10^{13} cm^{-2} and a Hall mobility of 750 cm^2/V · s. The mobility in the sidewall access regions is higher than that reported in [7] because of reduced dopant and interface scattering [14] in the graded back-barrier devices. The lower sheet resistance in the sidewall access regions compared to the previously reported E-mode devices reduces the contribution of the sidewall access regions to the source resistance. Transmission line measurements on the regrowth region gave a low sheet resistance of 100 Ω/□ for the n^{++} InGaN/InN regrowth layer and a lateral contact resistance of 5 Ω · μm between Ti and InN.

The pinchoff and the output resistance of the device are significantly better than those of the previously reported E-mode devices [7]. Fig. 4(a) shows that, at $V_{ds} = 4.0$ V, the $I_{on}(V_{gs} = 5.0\text{ V})/I_{off}(V_{gs} = 0.0\text{ V})$ is 1.16×10^4, while the I_{on}/I_{off} is 74 for the devices reported in [7] under similar bias conditions. The three-terminal breakdown of the device [Fig. 4(b)] is 8.6 V at $V_{gs} = 0$ V. Fig. 5 shows the output characteristics of a self-aligned N-polar E-mode device with 10-nm GaN channel and abrupt back barrier similar to the device in [7]. The gate length of the device is 120 nm, which is comparable to the gate length of the device in Fig. 2. The device shown in Fig. 2 with graded back barrier has better saturation and pinchoff characteristics compared to the device in Fig. 5 without graded AlGaN back barrier. These improvements are due to the reduced effect of the interface trap [8] in the graded back-barrier design compared to

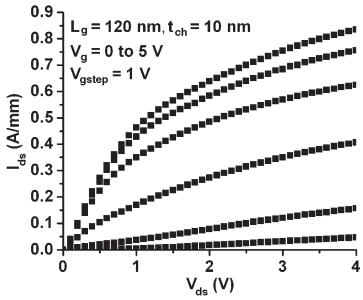

Fig. 5. DC characteristics of 10-nm GaN channel device without graded AlGaN back barrier and unoptimized InN regrowth condition.

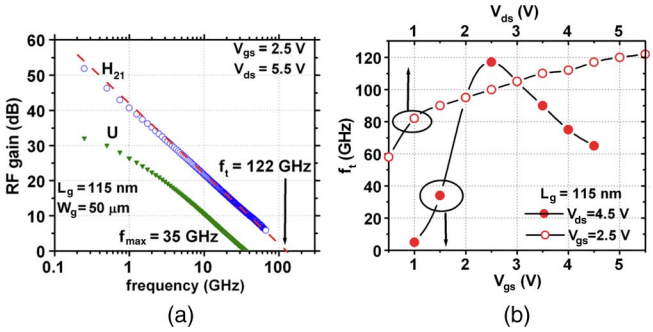

Fig. 6. (a) RF gains of the device versus frequency of the device shown in Fig. 2. An f_t of 122 GHz and an $f_{\max}$ of 35 GHz are extrapolated. (b) (Bottom x-axis, filled circles) f_t versus gate voltage for $V_{\rm ds} = 4.5$ V and (top x-axis, open circles) f_t versus drain bias for $V_{\rm gs} = 2.5$ V.

the AlN/GaN abrupt junction back-barrier design in Fig. 5 and in [7]. At $V_{\rm ds} = 4.0$, the maximum $I_{\rm on}/I_{\rm off}$ is 2.2×10^5, the OFF-state leakage limited by the gate leakage at $V_{\rm gs} = -1$ V. Lower subthreshold swing and leakage currents can be achieved by improving the dielectric–semiconductor interface. These devices are fully passivated because of the absences of surfaces near high-field regions of the device and hence do not show any current collapse in 200-ns gate-lag measurement.

Small-signal RF measurement of the device was performed on an Agilent E8361A PNA. The system was first calibrated with LRRM routine on a standard substrate. After on-wafer open-short de-embedding, the extracted current-gain cutoff frequency of the device is 122 GHz [Fig. 6(a)] with an $f_t - L_g$ product of 14 GHz $\cdot$ μm at a gate bias of 2.5 V and a drain bias of 5.5 V. The peak f_t of the device shown in Fig. 5 is 75 GHz. The improvement in $f_t - L_g$ product for the device in Fig. 2 is because of the low source access resistance and higher output resistance, which are the results of the optimized regrowth condition and graded back-barrier design, respectively. Fig. 6(b) shows the variation of f_t with gate bias and drain bias. There is no drop in f_t with increasing drain bias because of the absence of drain delay in the self-aligned structure. The $f_{\max}$ of the device is 35 GHz, which is low due to the highly resistive thin W-gate metal. Using a post regrowth top-gate process with low resistivity Au metal would lead to higher $f_{\max}$.

IV. Conclusion

In conclusion, we have demonstrated a vertically scaled 5-nm GaN channel E-mode MOS-HFET device with high dc and RF performance with low $R_{\rm on}$. Lateral scaling of the same device structure to sub-50-nm dimensions should lead to higher RF performance. Vertical scaling of the gate dielectric by using ZrO_2 and HfO_2 would further reduce the equivalent oxide thickness.

Acknowledgment

A portion of this work was performed in the UCSB Nanofabrication Facility, which is part of the NSF-funded NNIN network. The authors would like to thank A. D. Carter from Prof. Mark Rodwell's group at UCSB for sharing the ALD Al_2O_3 recipe.

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