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CMOS compatible integrated ferroelectric tunnel junctions (FTJ)

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Device Research Conference, June 21-24, 2015, Ohio State University

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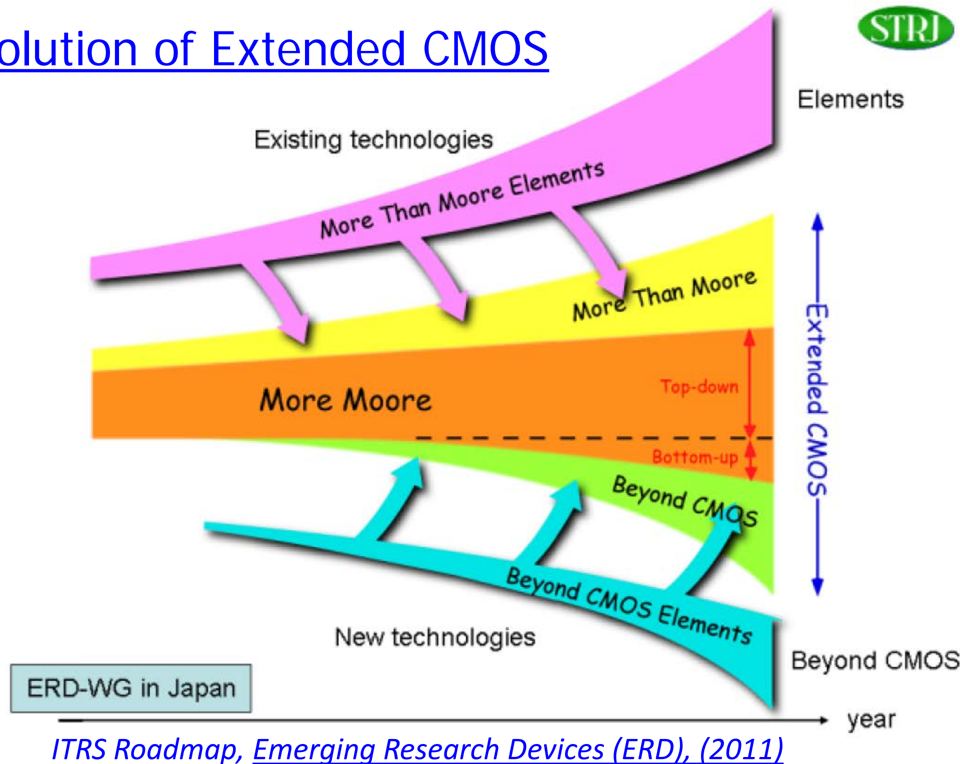
Outline

- Introduction and motivation
- Background and previous work
- Integrated FTJ device process
- Device results and discussion
- Conclusion

Motivation

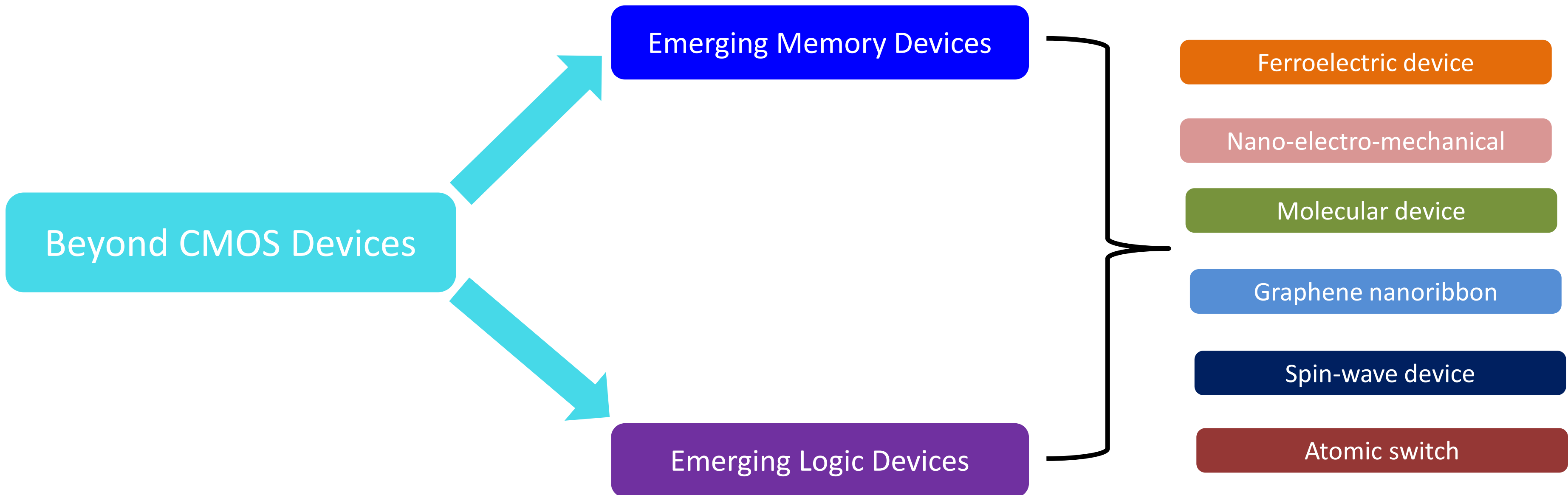


ITRS Roadmap, Emerging Research Devices (ERD), (2011)

Functional scaling of CMOS

- More Than Moore elements
- Beyond CMOS devices
- Non-charge based devices for beyond CMOS

Motivation

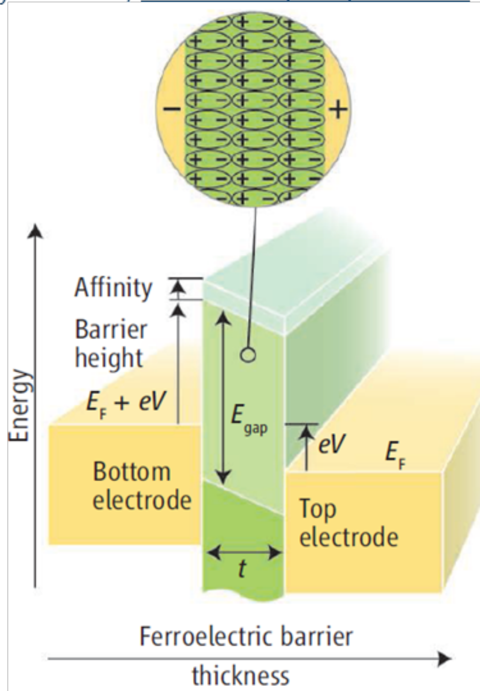


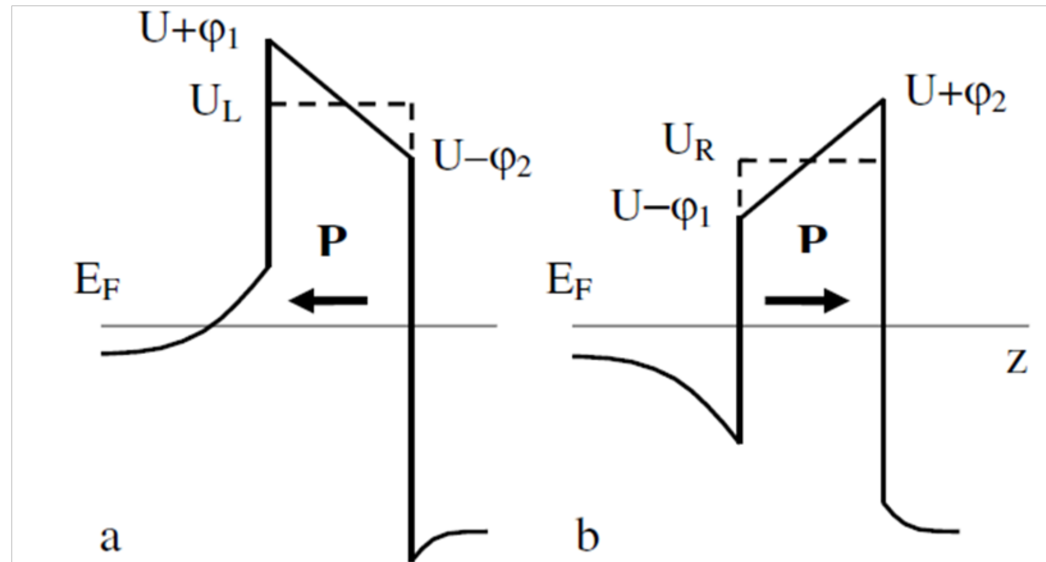
Beyond CMOS devices

- Exploit novel materials properties: spin, magnetic, ferroelectric
- Devices based on ferroelectrics : FE memory, FE FET, FE FTJ
- FE based devices for memory, logic, logic in memory

Ferroelectric tunnel junctions (FTJs)

Tsymbal *et al*, Science **313**(5784): 181-183.



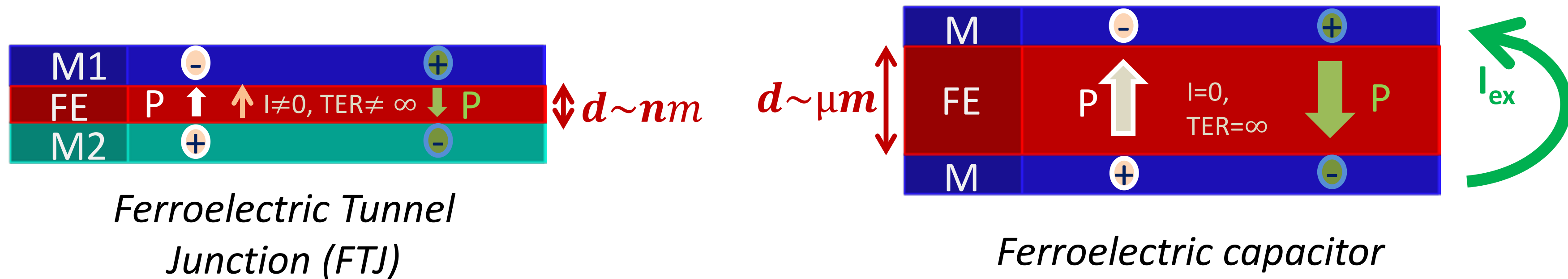


Zhuravlev, M. Y., *et al.* Physical Review Letters **94**(24): 246802.

Ferroelectric tunnel junction (FTJ) devices

- Tunnel current modulated by the polarization of FE material
- Large ON/OFF ratio
- Non-volatile state → novel FTJ based circuits

FTJ vs FeRAM



Ferroelectric Tunnel Junction (FTJ)

Ferroelectric capacitor

FTJ advantages:

- Non-destructive readout: based on measuring the tunneling conductance
- Good scalability: tunnel current can be measured for deep sub-μm junction
- Low read power: read voltage below V_c

Non-integrated FTJs

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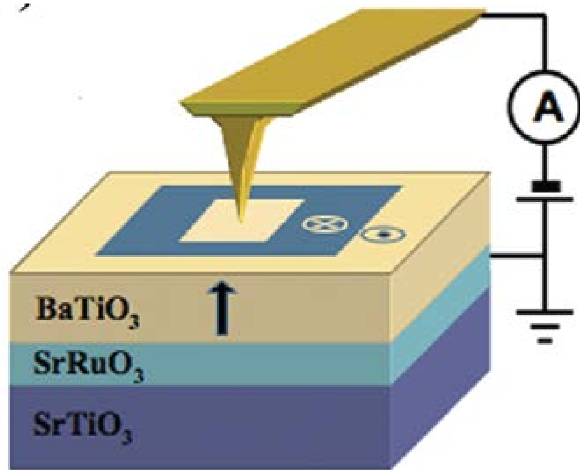
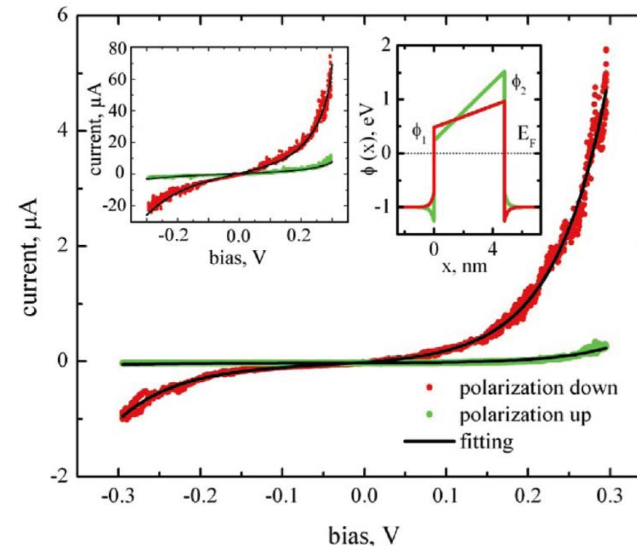
Gruverman, A., et al. (2009). Nano Letters **9**(10): 3539-3543.





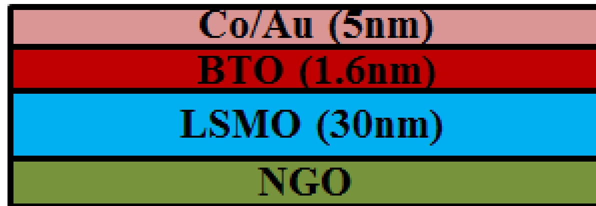
Non-integrated device using AFM tip as an electrode

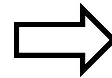
- Quick and fast technique to test device structures
- Hard to test scalability and CMOS compatibility
- Hard to do high speed switching tests

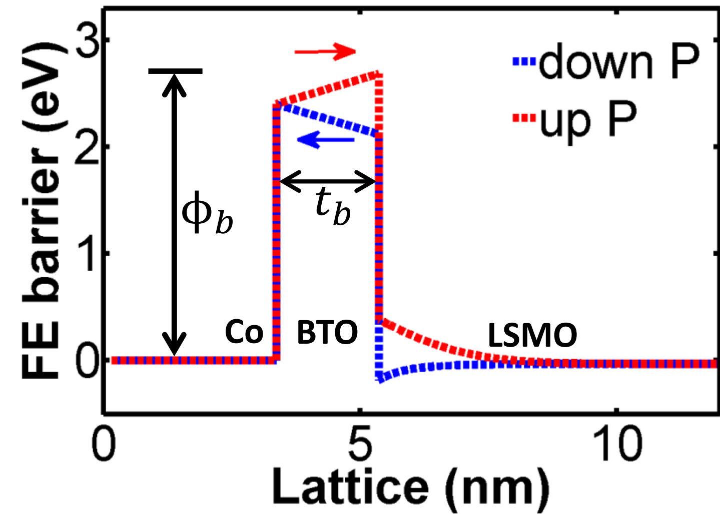
FTJ Integration required?

FTJ structure for integrated device

Atlas Silvaco simulation







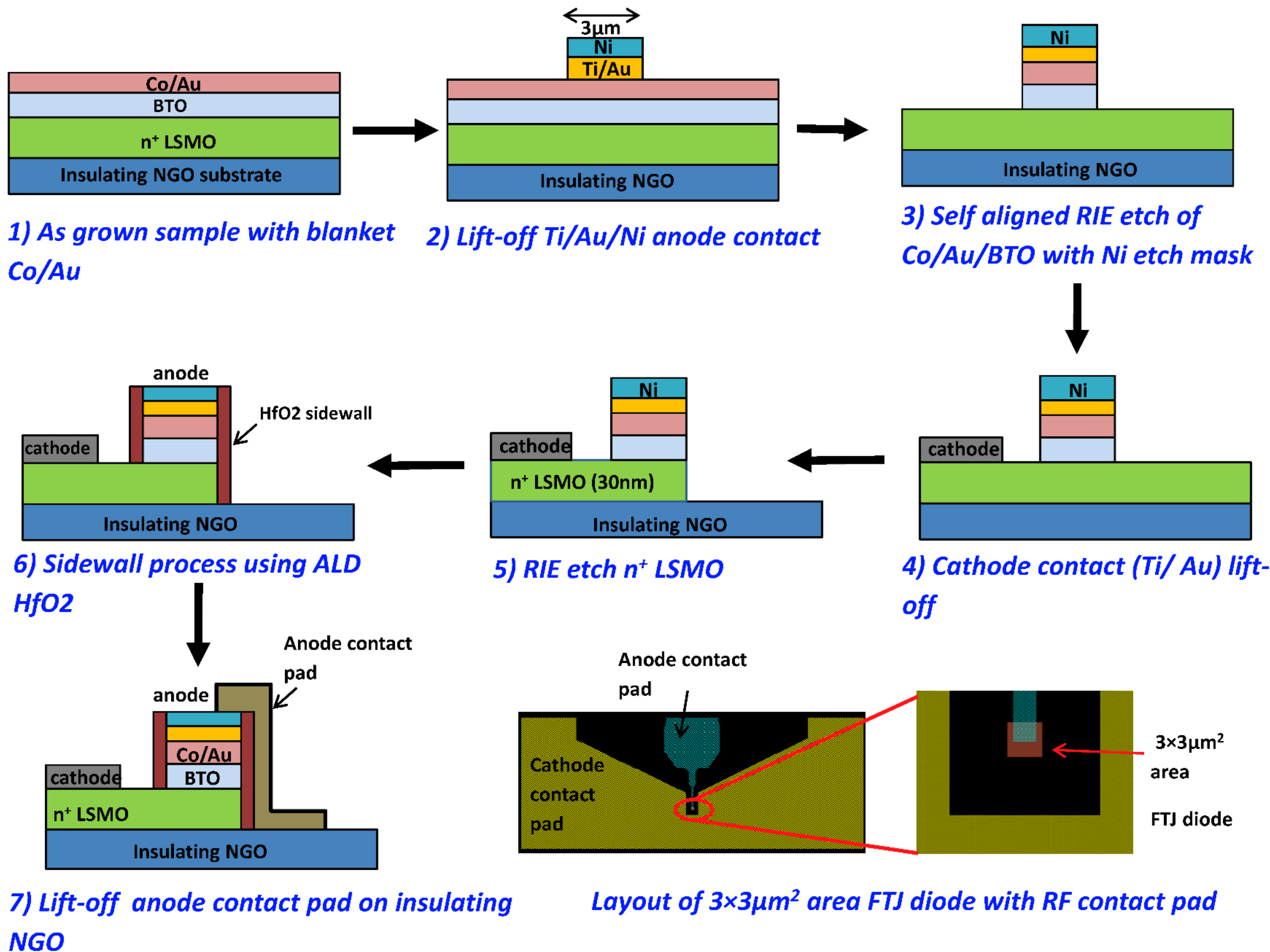
Electronic parameters of LSMO, BTO and Co used are E_{g_LSMO}=1 eV, E_{g_BTO}=3.3 eV, χ_{LSMO}=4.8 eV, χ_{BTO}=2.5 eV, ϕ_{CO} = 5eV .
$n^+ = 5\times10^{19}/cm^{-3}$

Energy band diagram of LSMO(30nm)-BTO(1.6nm)-Co(5nm) FTJ. ***$P=\pm40\mu C/cm^2$***

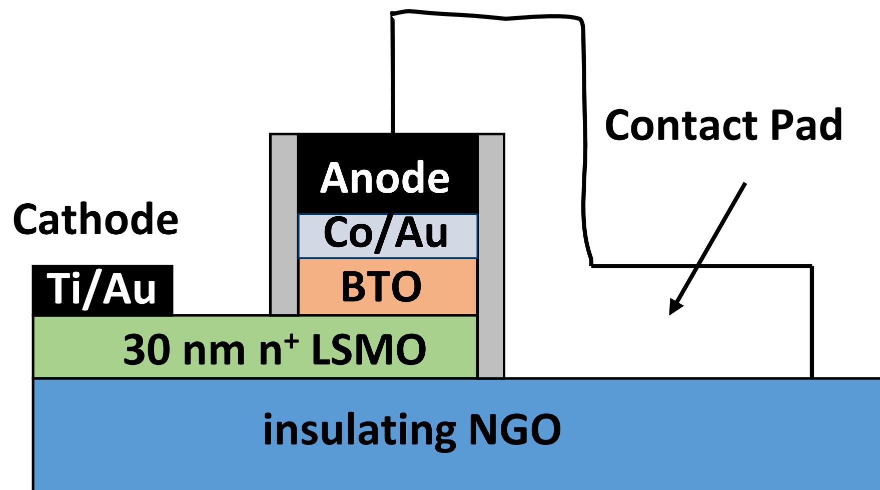
n-LSMO(30nm)-BTO(1.6nm)-Co(5nm) FTJ simulation:

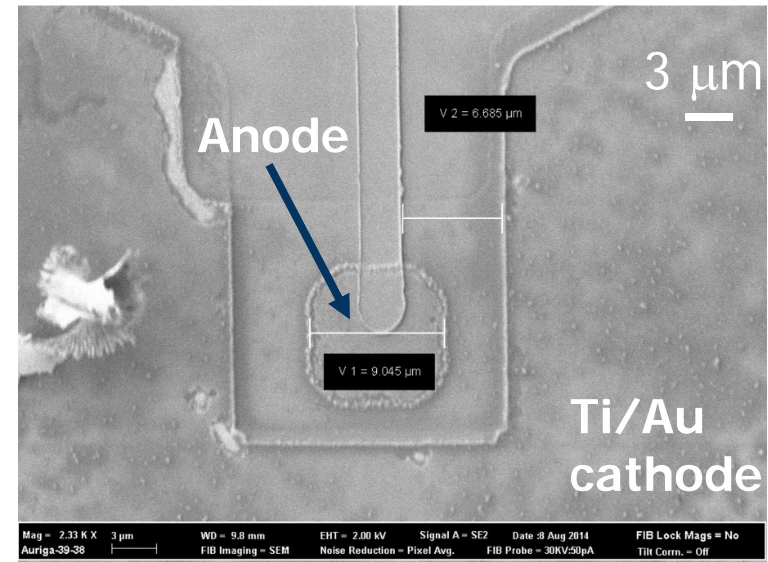
- FE barrier height (ϕ_b) changes from P↑ to P↓
- Effective tunnel barrier width (t_b) changes from P↑ to P↓
- Transmission probability modulated

Scalable FTJ process flow



FTJ Fabrication

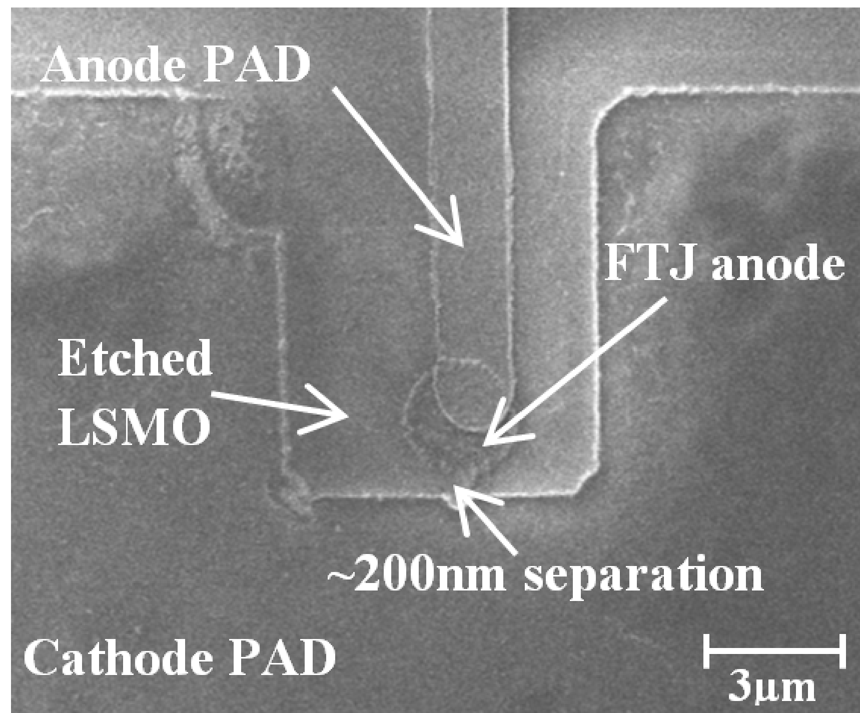


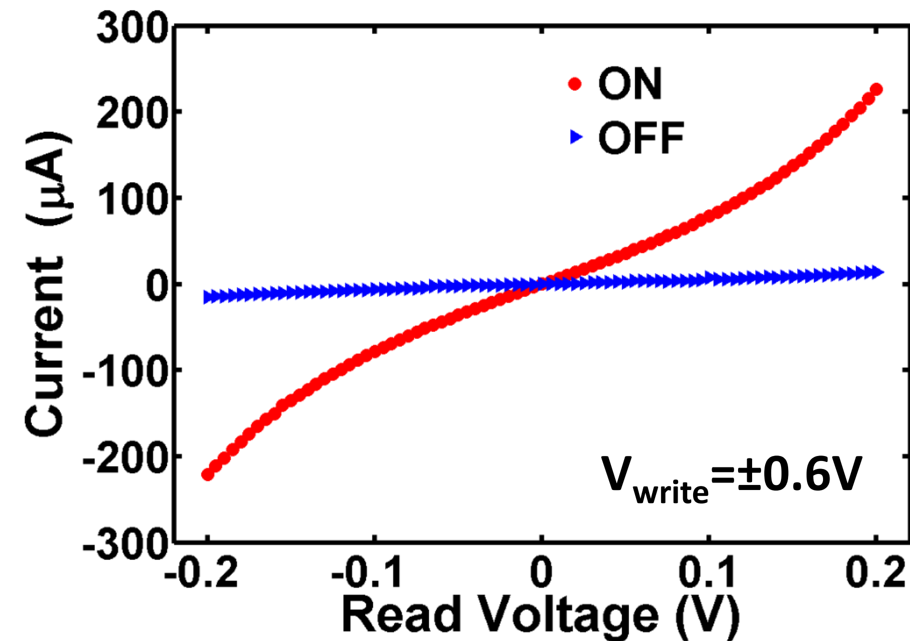


A fabricated FTJ

- FTJs fabricated with 4 unit cells of BTO
- Minimum device area 3 μm X 3 μm
- Process yield is good
- Devices show switching behavior

FTJ Switching

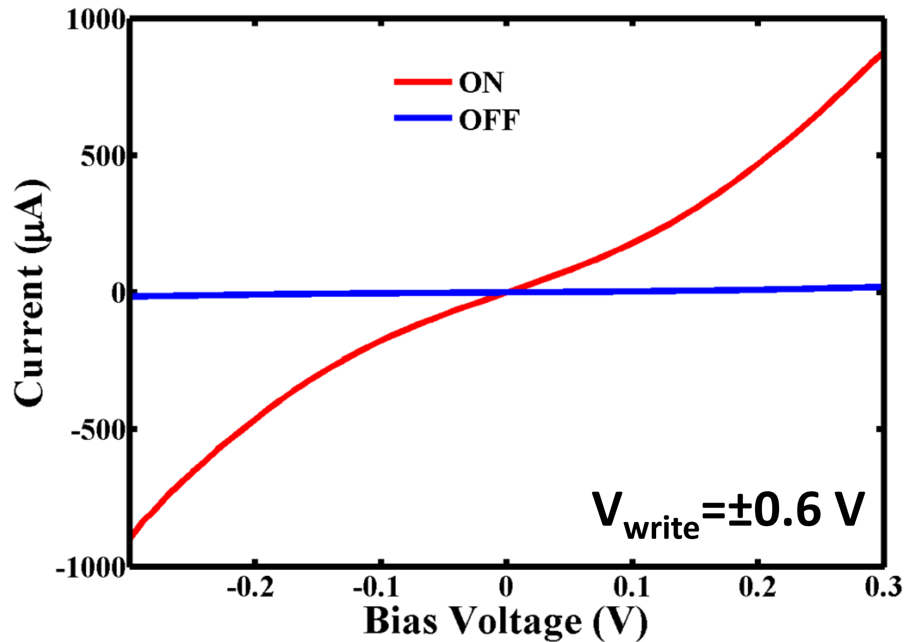




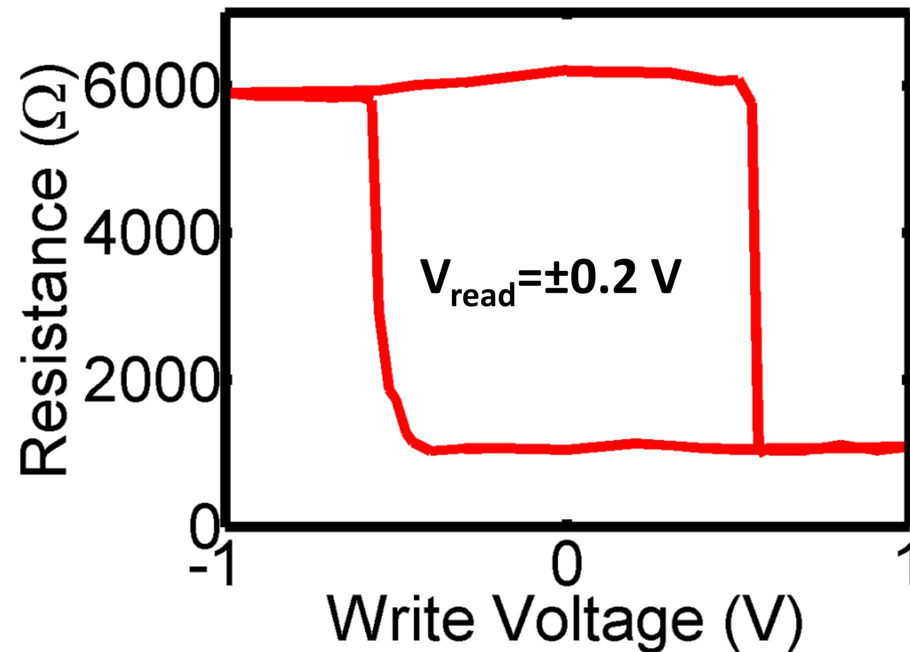
3 µm X 3 µm FTJ I-V

- Switching observed in 3 µm X 3 µm to 7 µm X 7 µm diodes
- Read voltage ±0.2V, write voltage ±0.6V~Low power operation

FTJ Switching



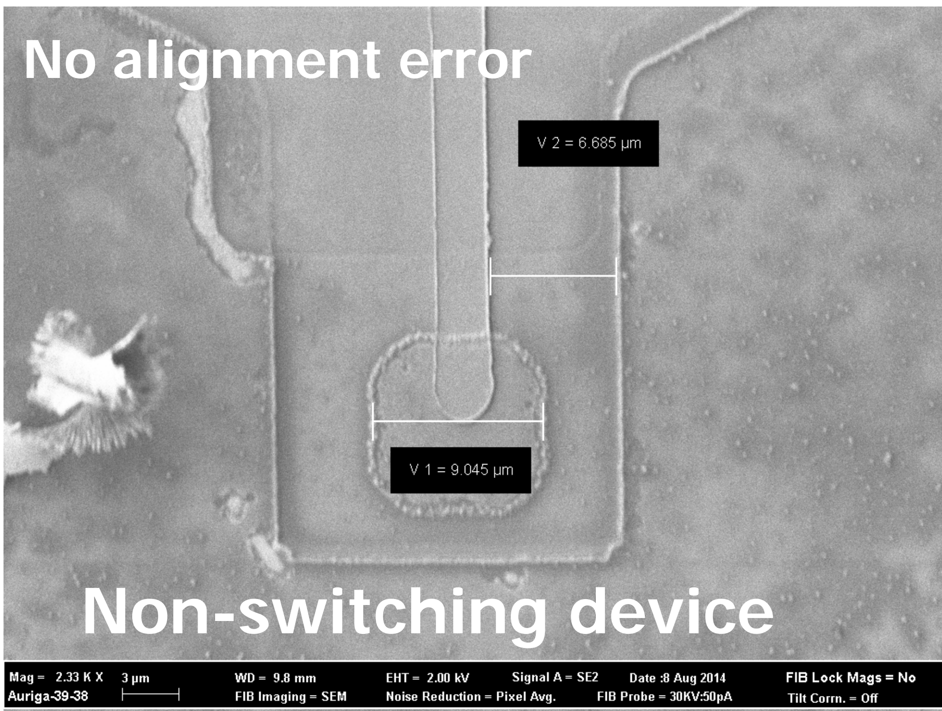
5 μm X 5 μm FTJ I-V

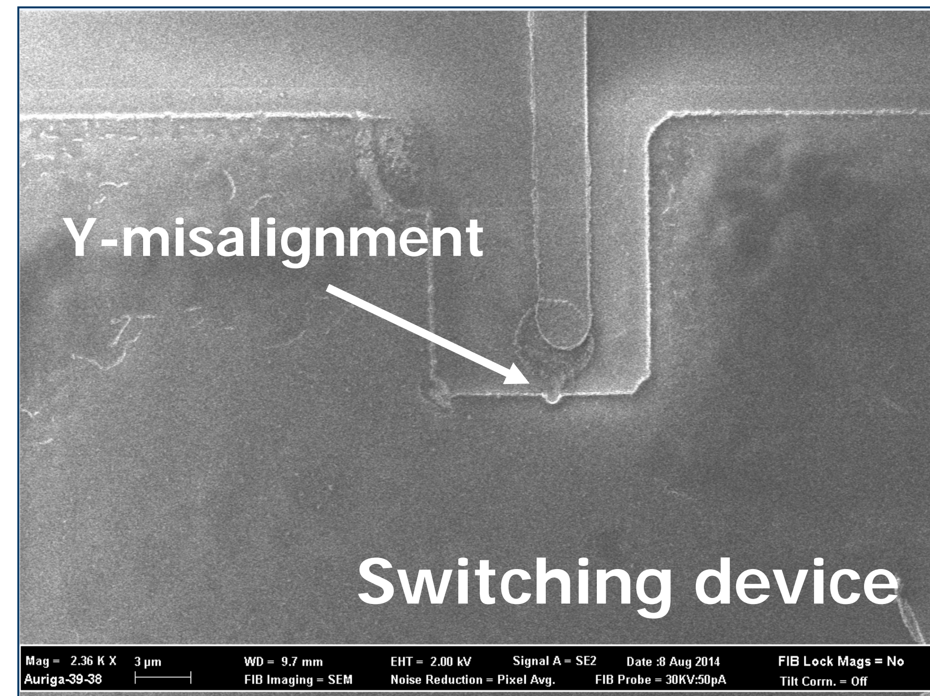


5 μm X 5 μm FTJ resistance loop

- Peak I_{on}/I_{off} = 60 observed in a 5 μm X 5 μm device
- Resistance loop is the fingerprint of FE polarization reversal
- Device switching yield is very poor (< 10 %)

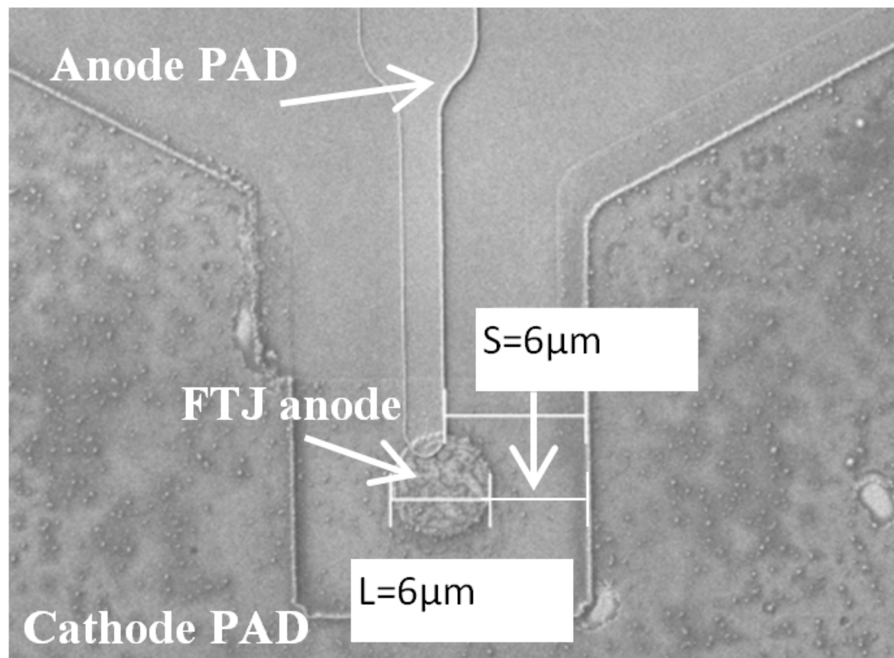
FTJ device yield



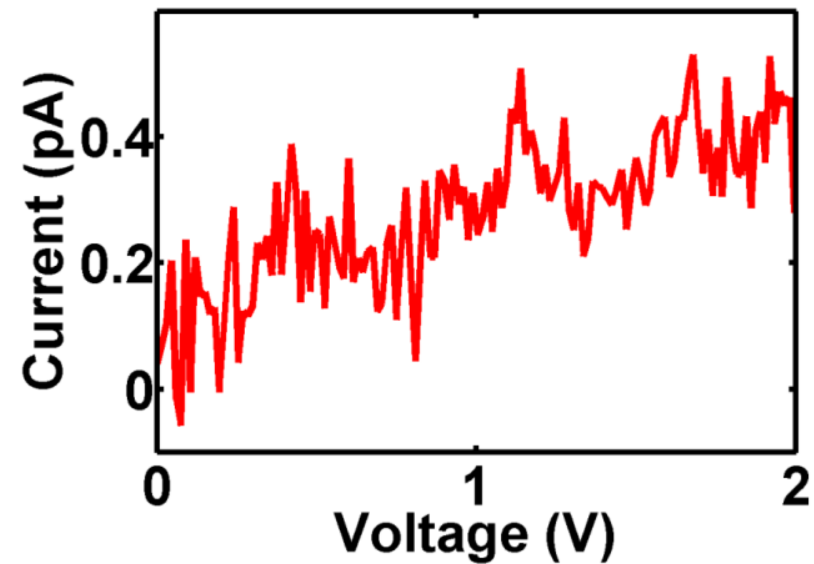


- Devices that show switching were misaligned
- Devices with good alignment show insulating behavior

Non switching FTJs



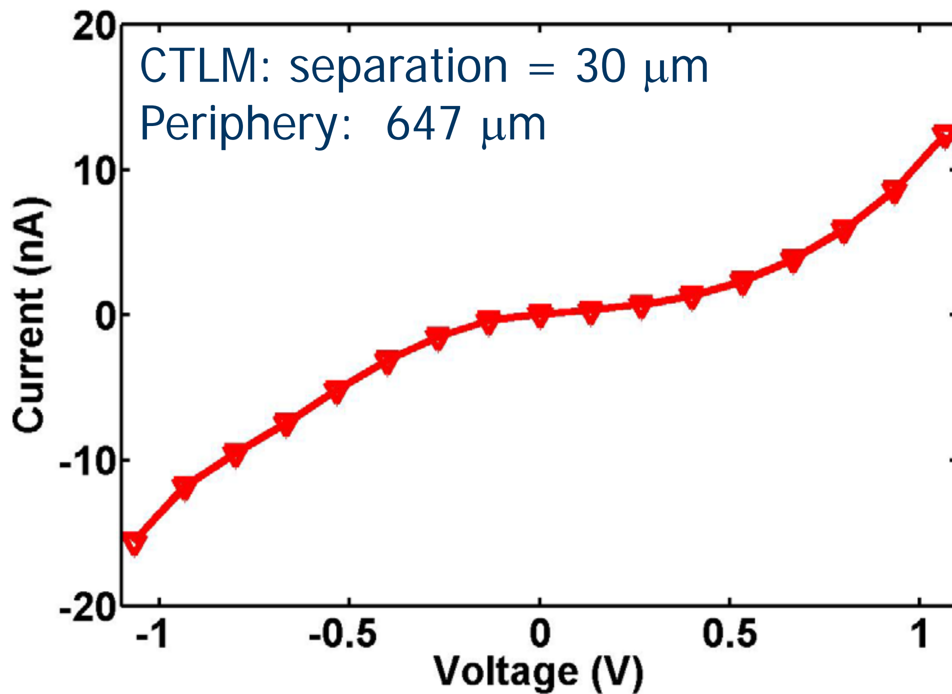
SEM of an FTJ with no switching



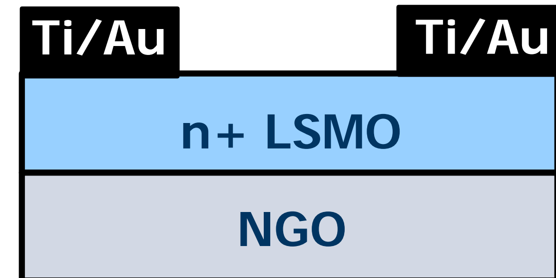
I-V of a non-switching device

- Good lithography alignment
- Minimum access length >5µm along X & Y-direction
- large parasitic resistance (>TΩ) on LSMO along X & Y-direction
- Applied voltage dropped across insulating LSMO

TLMs on n^+-LSMO



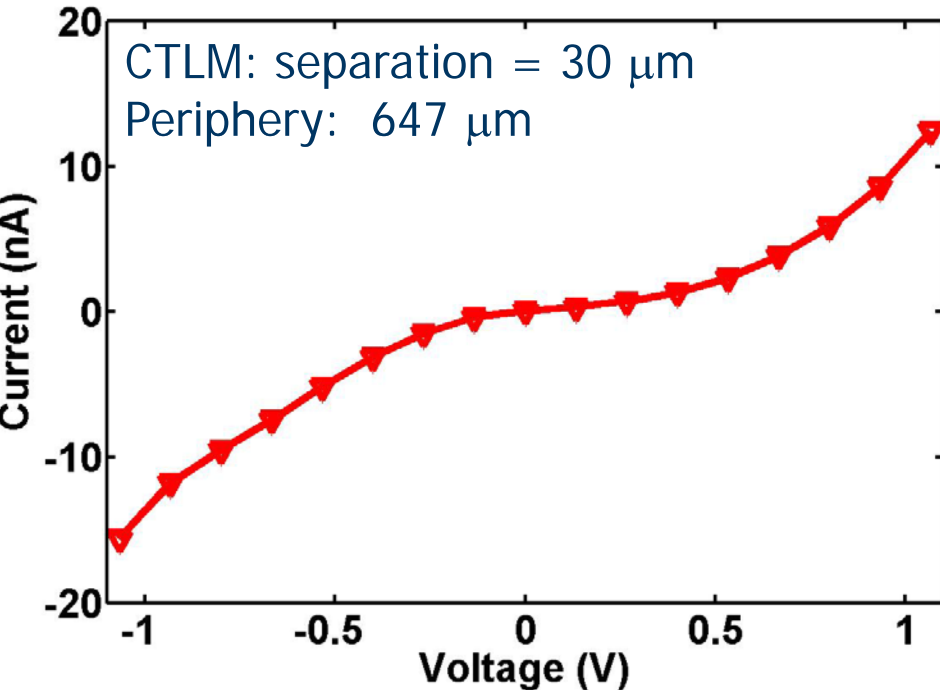
CTLM

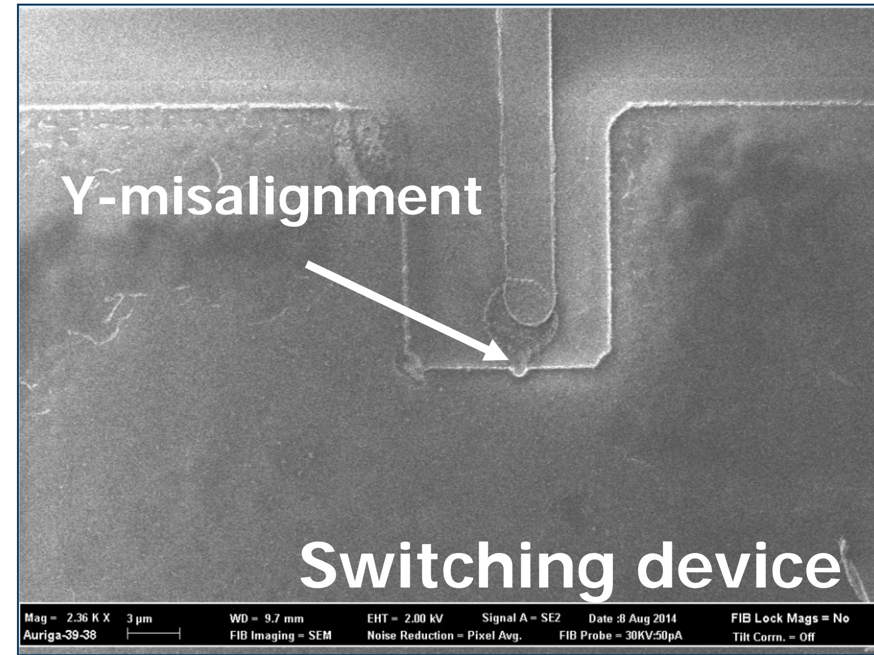


TLM structure after RIE etch of Co/Au and BTO

- High resistance observed on LSMO layer
- Bad contact with Ti/ LSMO
- Damage due to RIE

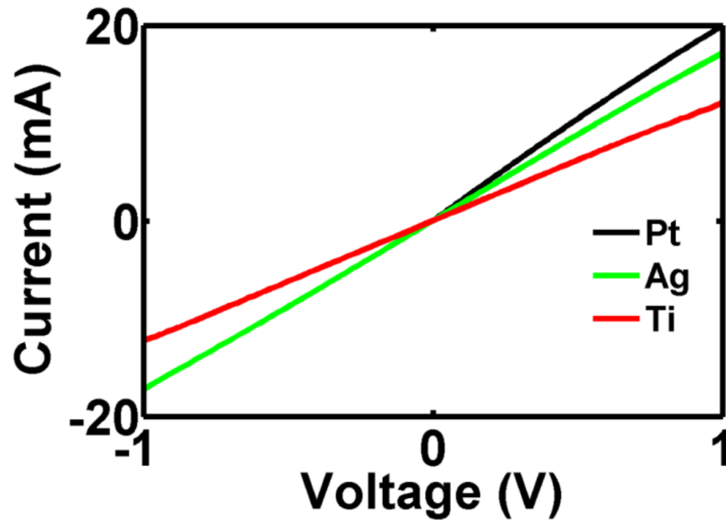
FTJ device yield



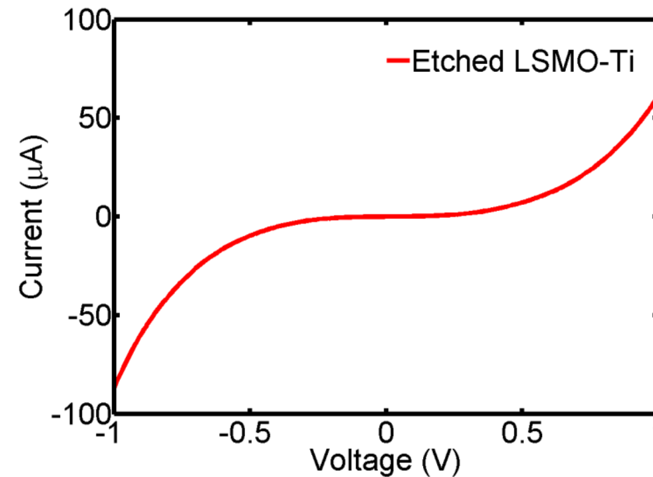


- High resistance observed on LSMO layer
- Misaligned device → reduced resistance → FTJ switching
- Devices with good alignment → high resistance

n^+-LSMO contact properties



Bare LSMO



After RIE and O_2 plasma

- Pt/Au, Ag, and Ti/Au TLM structure on bare LSMO
- All the metal layers show good ohmic behavior
- LSMO layer exposed to RIE process
- Ti contacts after RIE/O_2 plasma show high resistance

SRO electrode instead of LSMO

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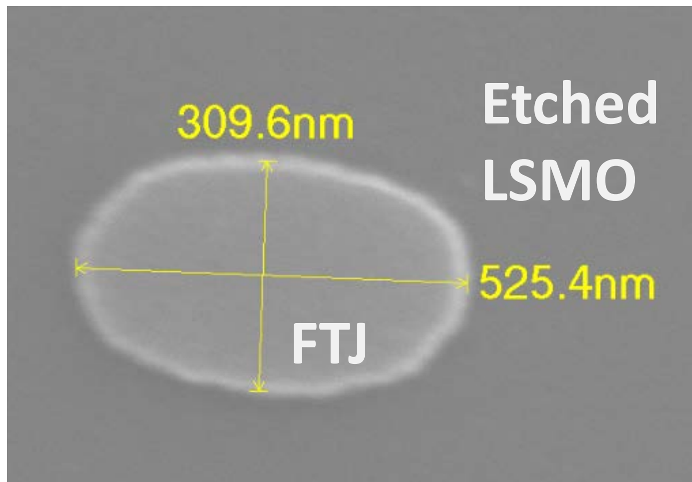
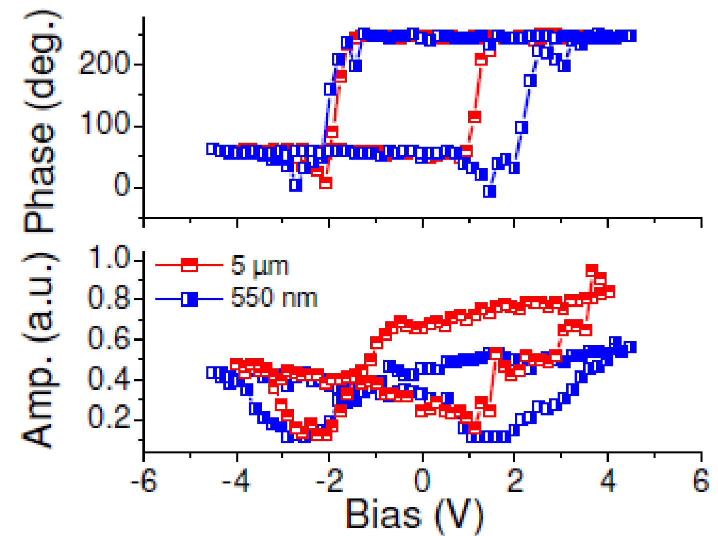
Sub-micron FTJ



Sum-micron FTJ without contact PAD



- Sub-micron anodes fabricated by electron beam lithography
- FTJ characteristics measured by AFM
- Devices show polarization loop

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Conclusion and future work

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- Integrated FTJ process demonstrated
- FTJ switching in integrated process
- Sub-micron dimension FTJ processed
- Contact degradation of etched LSMO layer
- Need FTJ electrode →SRO
- Integrate FTJ with SRO electrode future

Acknowledgement:

Semiconductor Research Corporation (SRC)