CMOS compatible integrated ferroelectric tunnel junctions (FTJ)

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As traditional CMOS scaling reaches fundamental limits, there is an increasing interest in non-charge based beyond CMOS devices that could increase the functionality of logic chips [1]. Ferroelectric tunnel junction (FTJ) devices are attractive due to their large ON/OFF ratios, non-volatile, and low energy operation [2]. Switching has been demonstrated in the metal-ferroelectric-metal (M-F-M) FTJs in non-integrated devices that use the conductive atomic force microscope (AFM) tip as an electrode [3-4]. However, it is necessary to investigate the CMOS compatibility, scalability, switching speed and switching dynamics in an integrated FTJ device. We report a CMOS compatible integrated FTJ fabrication process that is scalable from micron to deep submicron dimensions. The first generation integrated FTJs show switching with peak ON/OFF ratio of 60. We also report the scalability of the ferroelectric polarization loop to 550 nm x 550 nm device. Conductivity degradation of the $La_xSr_{1-x}MnO_3$ (LSMO) bottom conductor is observed due to reactive ion etch (RIE) process that impacts device performance.

The tunnel transmission coefficient is modulated in FTJ by changing the polarization of the ferroelectric barrier leading to ON and OFF state (Fig. 1). The cross-section of the FTJ device, LSMO/$BaTiO_3$ (BTO)/Co/Au, is shown in Fig. 2(a), LSMO and BTO layers were epitaxially grown on insulating (110) $NdGaO_3$ (NGO) substrates by pulsed laser deposition (PLD) technique. The Co (5 nm) /Au (10 nm) top metal layers were deposited by electron beam deposition. The conductive *n*-doped LSMO (30 nm) is the metal, BTO (4 unit cells ~ 1.6 nm) is the ferroelectric tunnel barrier and Co/Au is the top metal in the M-F-M FTJ structure. Fig. 2 shows the details of the fabrication process of the integrated FTJ device. First, Ti/Au/Ni anode contacts are defined by photolithography and lift-off. Next, using Ni as the etch-mask, Co/Au and BTO layers were etched using BCl_3/Ar based RIE (Fig. 2-c). Ti/Au cathode contacts are formed on the LSMO layer (Fig. 2-d). Self-aligned HfO_2 sidewalls are formed before defining the anode pads on the insulating NGO substrate (Fig. 2-e). The sidewalls prevent any anode pad to LSMO leakage current (Fig. 2-f).

The scanning electron micrograph (SEM) of a finished device is shown in Fig. 3. I-V measurement of FTJ was carried out using HP4155B semiconductor parameter analyzer. Fig. 4 shows the I-V characteristics in the ON and OFF state. A peak ON/OFF ratio of 60 is measured. The read voltage was ±0.2 V, and write voltage was ±0.6 V. Even though switching is observed, the switching yield was poor ~ 5%. Most devices show high resistance insulating (R > TΩ) behavior with no switching. I-V characteristics of TLM structures defined on *n*-doped LSMO layer also shows high resistance insulating behavior (Fig. 5). The SEM inspection of devices show that devices which were misaligned during lithography (access length < 200 nm) exhibit switching, whereas perfectly aligned devices (access length ~ 6 μm) show high resistance insulating behavior (Fig. 6). This can be explained from observed high resistance of LSMO layer; in the misaligned devices the parasitic resistance is reduced and the applied voltage is dropped across the intrinsic FTJ leading to switching while due to the large parasitic resistance in aligned devices the intrinsic device does not see the applied voltage. Fig. 7, shows the I-V characteristics of TLM structures on bare LSMO before and after being exposed to RIE which clearly shows the degradation of the conductivity due to RIE. Fig 8, shows the ferroelectric polarization loop measured by piezoresponse force microscopy (PFM) on anodes defined by lift-off and RIE, it clearly shows the existence of ferroelectric behavior in 550 nm x 550 nm device. An alternative to LSMO for FTJs is $SrRuO_3$ (SRO), I-V measurements on SRO before and after RIE show low resistance ohmic behavior that makes it a suitable choice for future integrated FTJ devices.

In summary, we developed a CMOS compatible scalable fabrication process of integrated FTJ devices that show switching. The conductivity degradation of LSMO layer after RIE was found to be a challenge for integrated devices. A SRO bottom conductor as the bottom metal in the M-F-M structure is suitable as it does not show conductivity degradation with RIE. Scalability of the ferroelectric behavior is demonstrated in 550 nm x 550 nm devices. These findings pave the pathway for scaling integrated FTJs to sub-100 nm dimensions.

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[1] ITRS Roadmap, Emerging Research Devices (ERD), (2011)
[2] E.Y. Tsymbal and A. Gruverman. *Nature Materials*, Vol. 12, 602-604, (2013)
[3] A. Gruverman, et al. *Nano Letters*, Vol. 9, 3539-3543, (2009)
[4] Z. Wen, et al. *Nature Materials*, Vol. 12, 617-621, (2013)

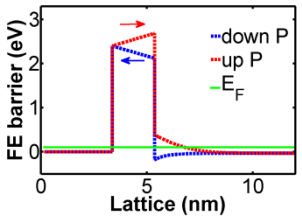

Figure 1: Simulated conduction band diagram of metal-ferroelectric-metal (MFM) FTJ device. The device structure is Co (5 nm)/ BTO (~2 nm)/ *n*-doped LSMO (30 nm). (E_{g_LSMO}=1 eV, E_{g_BTO}=3.3 eV, χ_{LSMO}=4.8 eV, χ_{BTO}=2.5 eV).

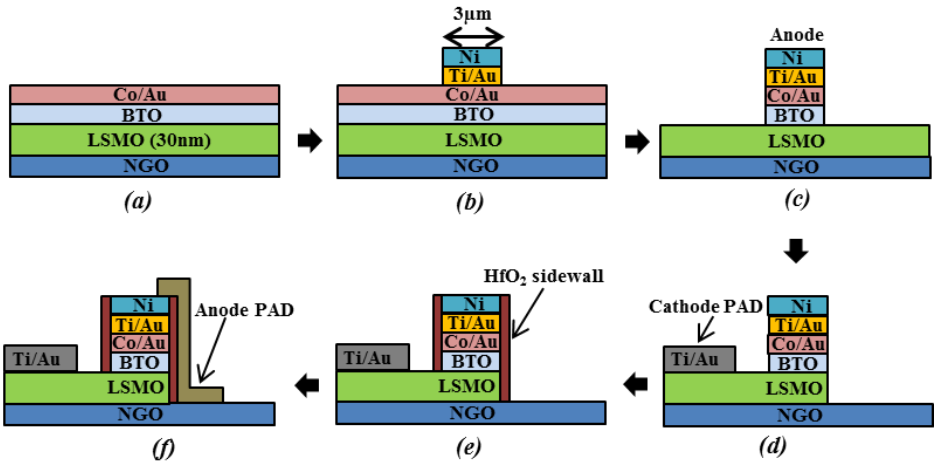

Figure 2: Fabrication process flow of FTJs.

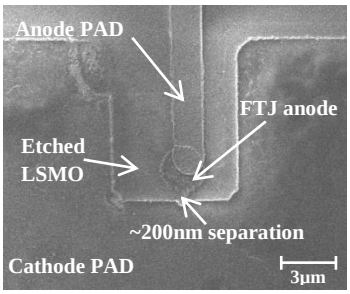

Figure 3: SEM image of finished device that exhibits switching. The misalignment in the y-direction leads to a smaller access distance (~200nm) between the intrinsic device and cathode contact pad.

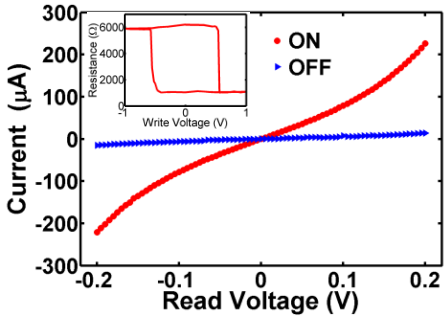

Figure 4: Switching I-V characteristics of 3×3µm^2 FTJ with on-off-ratio~60. The inset shows the resistance loop of the switching cycle.

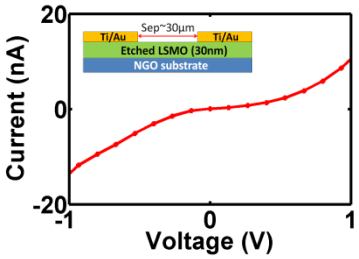

Figure 5: I-V on circular TLM (CTLM) structures defined on the FTJ wafer. Low current is observed indicating degradation of the conductivity of the *n*-doped LSMO layer.

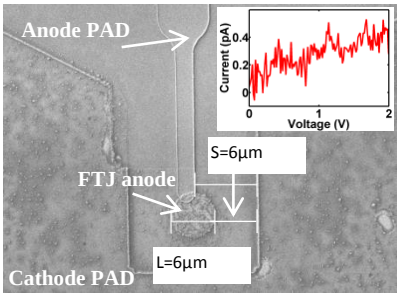

Figure 6: SEM of a device with no lithographic misalignment. Cathode pad to anode separation, S=6µm. Inset: IV of the device (L=6µm) showing high resistance. No switching is observed in these devices.

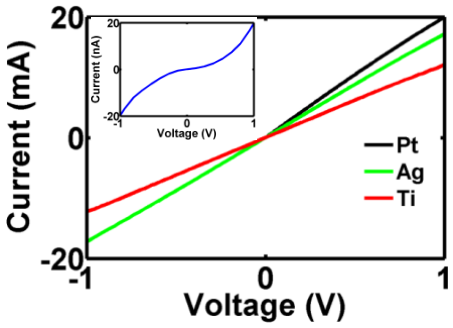

Figure 7: I-V characteristics on CTLM structures defined on 50 nm thick LSMO layer that has not been exposed to RIE. Ag, Pt, and Ti contacts show low resistance ohmic behavior. The inset shows I-V measurement on CTLMs (Ti contacts) after the LSMO layer was exposed to RIE process. Conductivity degradation is observed due to RIE.

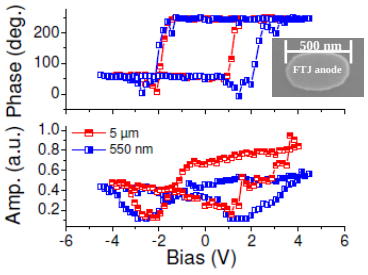

Figure 8: Ferroelectric hysteresis loop measured by PFM on micron and sub-micron FTJs (Co/Au/BTO (8 unit cells) /LSMO) showing the scalability of ferroelectric polarization loop to small area devices. Inset: SEM of submicron FTJ without contact PAD.