Depletion and Enhancement Mode β-Ga_2O_3 MOSFETs with ALD SiO_2 gate and near 400 V Breakdown Voltage

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As a next generation wide bandgap semiconductor for power electronics, β-Ga_2O_3 (Ga_2O_3) has shown a lot of potential in recent studies. It has been reported to have high Baliga's Figure of Merit (BFoM), a figure of merit for power devices, next only to diamond among wide bandgap semiconductor materials [1]. Moreover, a mature growth technology for large area substrates is a major practical advantage for cost effectiveness and rapid adaptation by industry [2]. Because of the advantages of this material, depletion mode MOSFETs and Schottky diodes based on Ga_2O_3 with high breakdown voltages have been recently demonstrated [3][4]. However, enhancement mode MOSFETs are preferred in power electronics applications. All the previous work incorporated ALD Al_2O_3 as gate barrier due to its high dielectric constant. However, a recent study reported that SiO_2/Ga_2O_3 interface has a much bigger conduction band offset than that of Al_2O_3/Ga_2O_3 [5] which is preferred in MOSFET. In addition, SiO_2/Ga_2O_3 interface has a relatively low interface states density according to our recent data. These properties make SiO_2 an attractive gate dielectric for Ga_2O_3 power MOSFETs. Here, we first report depletion mode MOSFET on MBE grown Ga_2O_3 with an ALD SiO_2 gate. We also report the first successful enhancement mode MOSFET on β-Ga_2O_3. Both depletion mode and enhancement mode MOSFETs show near 400 V off state drain source breakdown voltage.

All the devices were fabricated on MBE grown Ga_2O_3 epitaxial layer on Fe-doped semi-insulating Ga_2O_3 substrate. A 200 nm Sn-doped Ga_2O_3 epitaxial layer was grown by ozone MBE. The MOSFET fabrication process flow is shown in Fig. 1. First, a blanket layer of 20 nm SiO_2 was deposited on the wafer by plasma enhanced ALD. Then, silicon dioxide layer in the source/drain (S/D) region was etched away by CF_4/O_2 based reactive ion etching (RIE). After a short BCl_3/Ar RIE treatment, Ti/Au S/D contact metal was deposited. The contacts were then annealed under N_2 atmosphere to make them ohmic. For the gate, Ti/Au electrodes were defined by standard photolithography and lift-off procedure for depletion mode MOSFET, while Pt/Au stack was used for enhancement mode devices. The cross-section schematic of the final MOSFET is shown in Fig .2.

The capacitance-voltage (C-V) characteristics of the MOSCAPs were measured with Agilent 4294A precision impedance analyzer and the MOSFET IV characteristics were measured with HP 4155B semiconductor parameter analyzer. Fig. 3 shows a C-V curve for enhancement mode device. The output current-voltage characteristics of depletion and enhancement mode MOSFET are shown in Fig. 4 and Fig. 6, respectively. Fig. 5 and Fig. 7 show the corresponding input transfer characteristics. In Fig. 5, from the intercept of linear curve with *x*-axis, threshold voltage is ~ -4V for the depletion mode device with Ti/Au gate stack. While, the extracted threshold voltage from Fig. 7 is 3V for the enhancement mode device with Pt/Au gate stack. The on current for the depletion mode and enhancement mode devices are 48.7μA (V_{gs} = 12 V, V_{ds} = 30V) and 45μA (V_{gs} = 8 V, V_{ds} = 30V) respectively. The ON/OFF ratio for both devices is ~10^6. The drain source breakdown voltage in off state of the devices are 399 V and 390 V respectively for the depletion mode and enhancement mode devices. Both devices show similar breakdown voltages due to the same gate to drain spacing.

The on state drain current is limited by the high parasitic source/drain resistance. The TLM structures show a show high resistance with linear behavior. This high source/drain resistance is due to the low doping density in the epitaxial layer. The extracted active doping density from the C-V curve in Fig. 3 is $6.34\times10^{15}/cm^3$ which is lower than the target doping of ~$10^{17}/cm^3$, which increases both the contact resistance and source access region resistance. Increasing doping density and incorporation of ion-implantation will reduce the source drain parasitic resistance.

In conclusion, we demonstrated a depletion mode MOSFET with SiO_2/Ga_2O_3 structure and also the first successful enhancement mode MOSFET on β-Ga_2O_3 with near 400 V drain source breakdown voltage, which is promising for future Ga_2O_3 power devices. Advanced devices structure with reduced parasitic source/drain resistance will enable low ON resistance and higher breakdown voltages.

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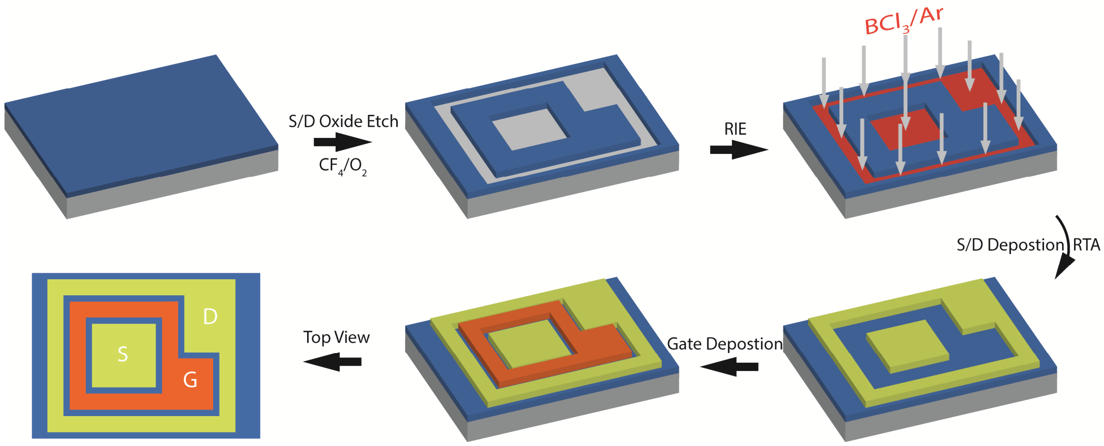

Fig. 1. Fabrication flow of Ga_2O_3 MOSFET.

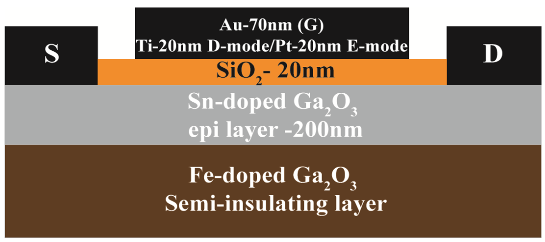

Fig. 2. Device layers and the cross-section schematic of depletion and enhancement mode Ga_2O_3 MOSFET.

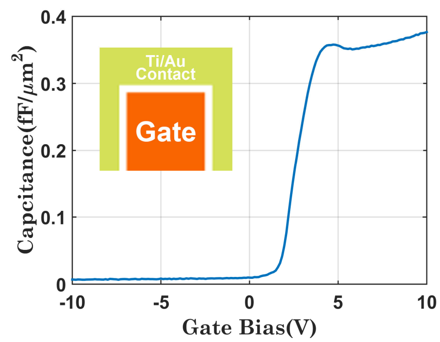

Fig. 3. Capacitance-Voltage characteristic of MOSCAP for enhancement-mode device.

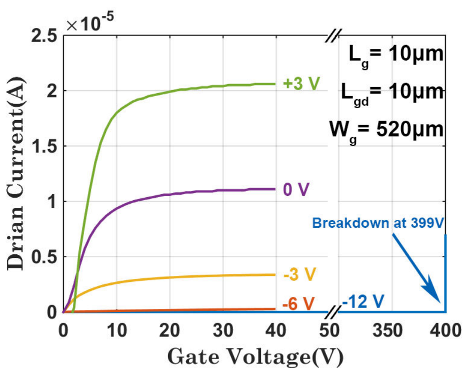

Fig. 4. Drain current- Voltage characteristic of depletion mode (D-mode) Ga_2O_3 MOSFET.

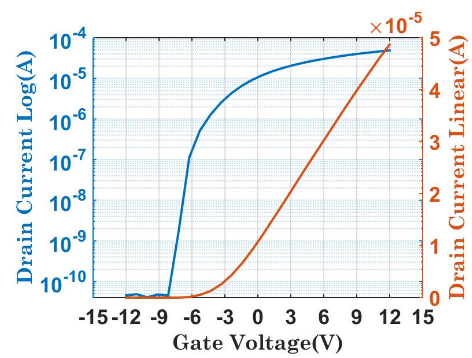

Fig. 5. I_{ds} vs. V_g for D-mode MOSFET at V_{ds}= 30V.

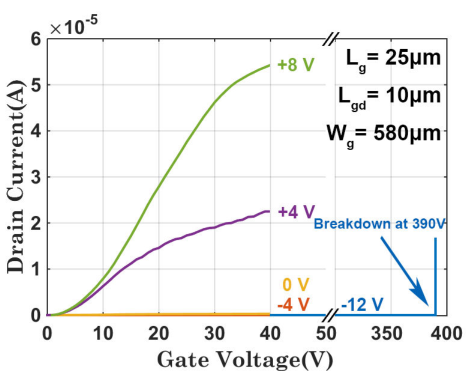

Fig. 6. Drain current- Voltage characteristic of Enhancement mode (E-mode) Ga_2O_3 MOSFET.

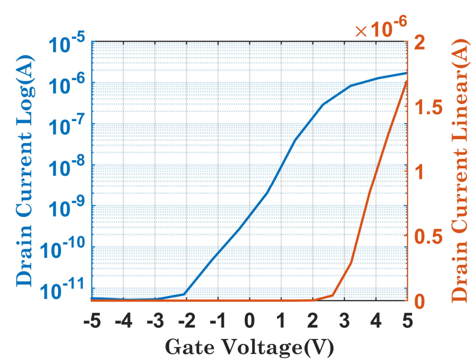

Fig. 7. I_{ds} vs. V_g for E-mode MOSFET at V_{ds}= 20V.