Spectroscopic and electrical calculation of band alignment between atomic layer deposited SiO_2 and β-Ga_2O_3 ($\bar{2}01$)

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The energy band alignment between atomic layer deposited (ALD) SiO_2 and β-Ga_2O_3 ($\bar{2}01$) is calculated using x-ray photoelectron spectroscopy and electrical measurement of metal-oxide semiconductor capacitor structures. The valence band offset between SiO_2 and Ga_2O_3 is found to be 0.43 eV. The bandgap of ALD SiO_2 was determined to be 8.6 eV, which gives a large conduction band offset of 3.63 eV between SiO_2 and Ga_2O_3. The large conduction band offset makes SiO_2 an attractive gate dielectric for power devices. © *2015 AIP Publishing LLC*.
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Recently, wide bandgap β-Ga_2O_3 (Ga_2O_3) has received much attention as an attractive semiconductor for power electronics and UV detector applications due to its large bandgap of 4.6–4.9 eV.[1–3] In addition, high bulk electron mobilities in Ga_2O_3 lead to a Baliga Figure of Merit (BFoM), which exceeds that of SiC and GaN,[4,5] which makes it as an attractive choice for next generation of power semiconductor devices. Moreover, large area bulk crystals of Ga_2O_3 can be grown using scalable crystal growth technologies.[6–10] Both doped and semi-insulating bulk crystals are available commercially.[4,5,11,12] Epitaxial growth of Ga_2O_3 by molecular beam epitaxy (MBE)[4,13,14] and ion implantation doping technology[15] has also been reported. All these factors make Ga_2O_3 a strong candidate for next generation power electronics. Ga_2O_3 metal-oxide semiconductor field effect devices (MOSFETs) with high breakdown voltages, large ON/OFF ratios, and high temperature operation have been recently demonstrated.[5,15–17] These devices use atomic layer deposited (ALD) Al_2O_3 as a gate barrier. The conduction band offset between Al_2O_3 and Ga_2O_3 has been determined to be 1.5–1.7 eV.[18,19] A higher conduction band offset is preferred to reduce thermal leakages during high temperature operation of power devices. However, the large bandgap of Ga_2O_3 limits the choice of gate dielectrics. In addition to be used as gate barrier, dielectrics are also used for passivation and electric field profiling by field plates in power semiconductor devices.

Silicon dioxide (SiO_2) is an attractive gate barrier material for Ga_2O_3 due to its large bandgap of $\sim$9 eV.[20] However, there is no report of the band parameters between SiO_2 and Ga_2O_3. In this letter, we report the band alignment between ALD SiO_2 and β-Ga_2O_3 ($\bar{2}01$). Silicon dioxide deposited by ALD has great potential to serve as a gate dielectric in Ga_2O_3 based power device because of the expected large conduction band offset at the interface of SiO_2/Ga_2O_3 and also because of its large critical breakdown electric field ($\sim$10 MV/cm (Ref. 21)). In this work, the conduction band offset of ALD-SiO_2/Ga_2O_3 hetero-junction was characterized using X-ray photoelectron spectroscopy (XPS) as well as the tunneling current through metal-oxide-semiconductor capacitors (MOSCAPs).

β-Ga_2O_3 ($\bar{2}01$) crystals studied here was grown at Tamura Corporation with an n-type doping (Sn doped) density of $\sim 9 \times 10^{18}/cm^3$. A surface root mean square (rms) roughness of 0.13 nm was measured by atomic force microscopy (AFM) on these wafers. For XPS characterization, a thin layer ($\sim$3 nm) of SiO_2 was deposited on Ga_2O_3 by plasma-enhanced ALD in an Oxford FLEXAL system at 300 °C with trisdimethylaminosilane (3DMAS) and O_2 plasma at 250 W. Standard solvent degreasing procedure was used to clean the wafers before SiO_2 deposition. For band offset calculation by XPS, core level spectra of Si in bulk SiO_2 are necessary. We use 40 nm thick SiO_2 on Si as the bulk standard. For electrical studies, a 40 nm layer of SiO_2 was deposited on Ga_2O_3. The growth rate was calibrated on silicon wafers to be 0.71 Å/cycle. For electrical characterization, the MOSCAP structure, shown in Figure 1, was fabricated. First, the top Ti/Au electrodes were defined by standard photolithography and lift-off technique. Next, the silicon oxide and Ga_2O_3 were etched by CF_4/Ar based reactive ion etching. And finally, the bottom Ti/Au electrodes are defined. The sample was then annealed at 300 °C for 1 h to reduce the contact resistance.[17]

XPS measurements were performed using a Physical Electronic PHI VersaProbe 5000 equipped with a hemispherical energy analyzer. A monochromic Al Kα X-ray source (1486.6 eV) was operated at 25.3 W and 15 kV. The energy of the analyzer was operated at a pass energy of 117.5 eV for survey acquisitions and 23.50 or 11.75 eV for high-resolution acquisitions. The energy resolution was 0.025 eV for high resolution spectra or 1.0 eV for survey spectra. The operating pressure of XPS was $<4 \times 10^{-6}$ Pa (3.0×10^{-8} Torr) and the

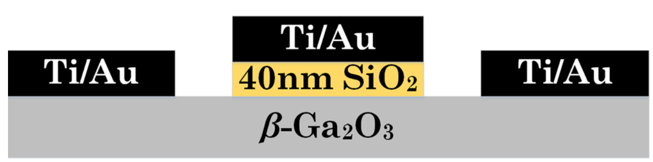

FIG. 1. Cross-section schematic of Ga_2O_3 MOSCAP device.

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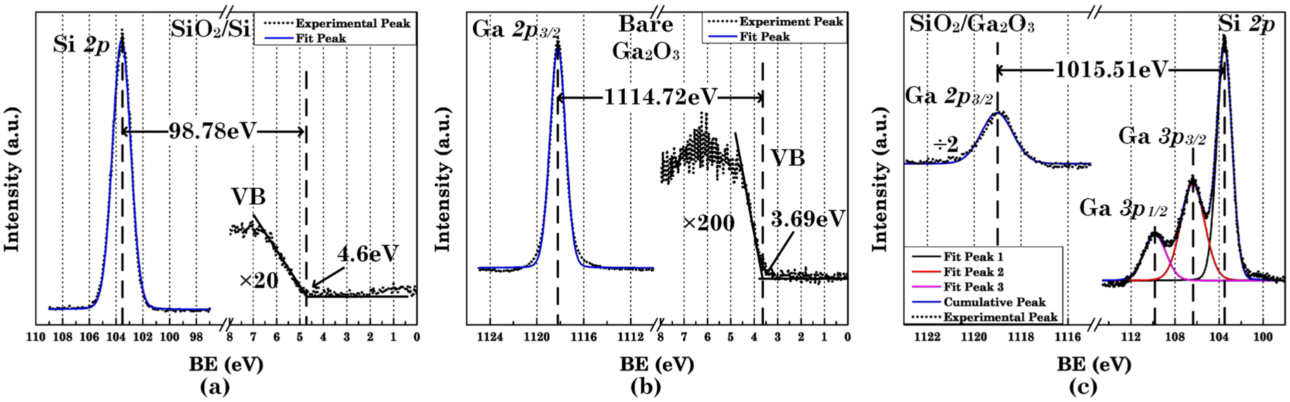

FIG. 2. XPS spectra used to calculate valence band offset. (a) Si *2p* peak and valence band maximum acquired from 40 nm SiO_2/Si. (b) Ga $2p_{3/2}$ peak and valence band maximum acquired from bare Ga_2O_3. (c) Ga $2p_{3/2}$ peak and Si *2p* peak obtained from SiO_2 (3 nm)/Ga_2O_3 heterostructure. Ga $3p_{3/2}$ and $3p_{1/2}$ peaks were also observed through SiO_2 layer as shown in (c). The VBO was calculated as 0.43 eV.

background pressure was $<1 \times 10^{-6}$ Pa (7.5×10^{-9} Torr). Dual charge neutralization was utilized to reduce the effects of charging on the acquired signal. Binding energies were calibrated by setting the CH_x peak in the C *1s* envelope at 284.8 eV to correct for charging effects.[18,22] However, the valence band offset (VBO) measurement is not sensitive to charging effects.

Figures 2(a)–2(c) show the XPS spectra for 40 nm SiO_2/Si, β-Ga_2O_3, and SiO_2 ($\sim$3 nm)/β-Ga_2O_3 structure. XPS results were curve fitted with a Gauss-Lorentzian band type with Shirley background subtraction[23–25] with curve fitting limits as follows: binding energy $\pm$0.4 eV, FWHM $\pm$0.2 eV, and % Gauss = 92%. The core level (Ga $2p_{3/2}$) spectra on bare Ga_2O_3 shows a single peak (1118.4 eV) corresponding to Ga-O bond.[18] The valence band maxima (VBM) were found by the linear extrapolation of the valence band states,[18,24,25] the VBM of Ga_2O_3 was found to be 3.69 eV above the Fermi level (E_F), as shown in Figure 2(b). For the SiO_2 (3 nm)/Ga_2O_3 sample, in addition to the Si-O bonds, the XPS spectrum shows the Ga *3p* peaks from underneath the ALD-SiO_2 layer. Next, the valence band offset was calculated by the following equation:[18,26]

$$\Delta E_v = (E_{Si2p}^{SiO_2/Ga_2O_3} - E_{Ga2p3/2}^{SiO_2/Ga_2O_3}) + (E_{Ga2p3/2}^{Ga_2O_3} - E_{VBM}^{Ga_2O_3}) - (E_{Si2p}^{SiO_2} - E_{VBM}^{SiO_2}),$$

where the subscripts indicate the XPS peak and the superscripts indicate the sample. From the measured XPS profiles, $(E_{Si2p}^{SiO_2/Ga_2O_3} - E_{Ga2p3/2}^{SiO_2/Ga_2O_3})$, $(E_{Ga2p3/2}^{Ga_2O_3} - E_{VBM}^{Ga_2O_3})$, and $(E_{Si2p}^{SiO_2} - E_{VBM}^{SiO_2})$ are -1015.51, 1114.72, and 98.78 eV, respectively, which gives a valence band offset (ΔE_V) of 0.43 eV. Figures 3(a) and 3(b) show core level and the loss structure of O *1s* on SiO_2/Si and bare Ga_2O_3 samples. From the loss peak, the band gap of Ga_2O_3 and SiO_2 was found to be 4.54 eV and 8.6 eV,[18,27] respectively. The conduction band offset is calculated by

$$\Delta E_C = \Delta E_g - \Delta E_V,$$

where ΔE_g is the band gap difference between Ga_2O_3 and SiO_2 and ΔE_V is the calculated valence band offset. Taking the band gap difference to be 4.06 eV, a conduction band offset of 3.63 eV is calculated.

In addition to XPS measurement, electrical characterization of the MOSCAPs was also carried out to calculate the conduction band offset between SiO_2 and Ga_2O_3. C-V characteristic of MOS diode is shown in Figure 4. Both first derivative of C-V and flatband capacitance method indicate a flatband voltage about 9.7 V, suggesting the existence of negative surface charge between SiO_2 and n-Ga_2O_3. An electron density of $9.7 \times 10^{18}\,cm^{-3}$ for n-Ga_2O_3 was estimated using differential capacitance-voltage profile technique,[28] which is given by

$$n(W) = -\frac{C^3}{qK_s\varepsilon_0 A^2 dC/dV} = \frac{2}{qK_s\varepsilon_0 A^2 d(1/C^2)/dV},$$

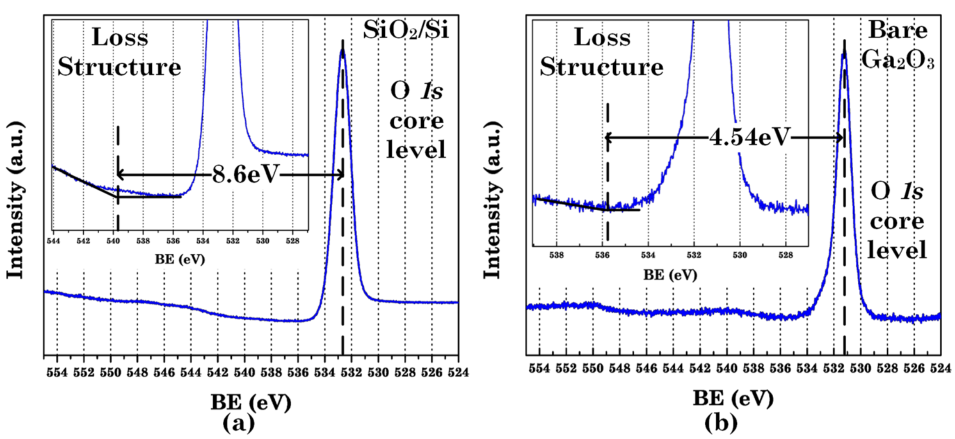

FIG. 3. O *1s* peaks obtained from (a) 40 nm SiO_2/Si and (b) bare Ga_2O_3 to determine bandgap of SiO_2 and Ga_2O_3. Inset of (a) and (b) shows the corresponding loss structure. The bandgap for SiO_2 and Ga_2O_3 is 8.6 eV and 4.54 eV, respectively.

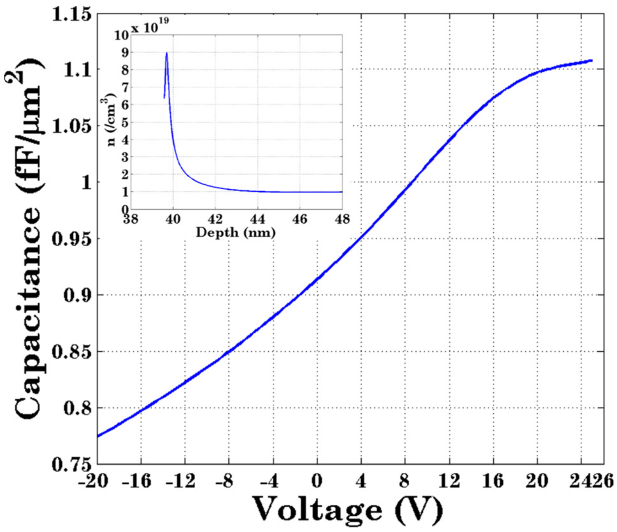

FIG. 4. C-V profile of Ti/SiO_2/β-Ga_2O_3 diode. Inset shows carrier density profile derived from C-V profile. The extracted doping density is $9.7 \times 10^{18}/\mathrm{cm}^3$.

$$W = \frac{K_s \varepsilon_0 A}{C},$$

where $n(W)$ is the carrier density, W is the depth from surface of metal and oxide, K_s is relative permittivity of the channel, and A is the area of contact. The current-voltage characteristics of the MOSCAP are shown in Figure 5. The current in the reverse bias is negligibly small (not shown), while in the forward direction current remains low till 50 V then rises rapidly due to Fowler-Nordheim (F-N) tunneling. Destructive breakdown of the MOSCAPs was observed at ~60 V both in the forward and the reverse bias conditions. We extract the conduction band offset from the F-N tunneling current in forward bias.[18] When sufficient forward bias is applied F-N tunneling takes place[29] as indicated in the inset of Figure 5. The F-N tunneling current which depends on ΔE_c is given by:[18,29]

$$J = \frac{q^3 m_0 E_{ox}^2}{8\pi h m_{ox} \Delta E_c} \exp\left[-\frac{8\pi\sqrt{2m_{ox}}}{3hqE_{ox}}(\Delta E_c)^{\frac{3}{2}}\right],$$

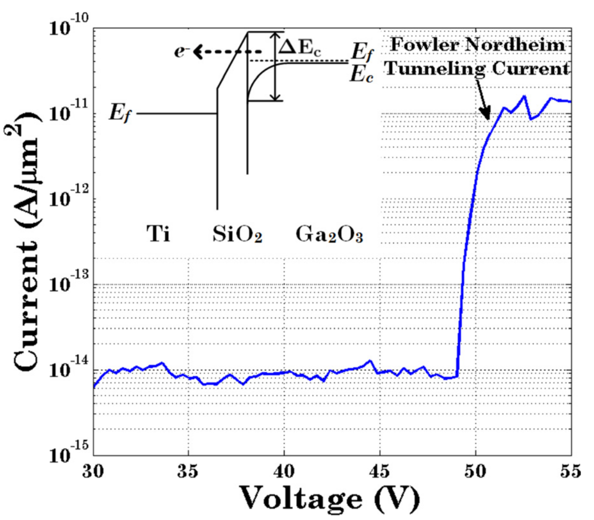

FIG. 5. I-V characteristic of MOSCAP at forward bias. The F-N tunneling region is indicated. Inset shows a schematic band-diagram, which enables F-N tunneling.

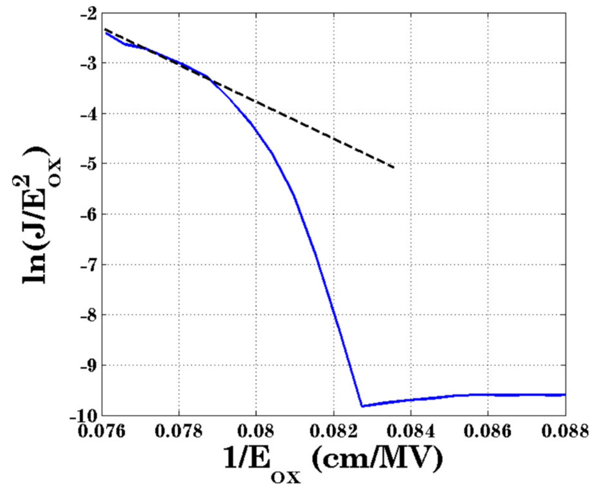

FIG. 6. $\ln(J/E_{ox}^2)$ vs. $1/E_{ox}$ plot derived from forward I-V plot in Fig. 5. In the F-N tunneling region, as indicated by the line, the measured slope is -3.1488×10^{10}.

where J is the current density, q is the electron charge, h is the Plank's constant, m_0 is the free electron mass, and m_{ox} is the electron effective mass in oxide. E_{ox} is the electric field strength in the oxide, which can be calculated easily if the diode is in the strong accumulation region at large forward bias voltages. ΔE_C was extracted from the slope (S) of $\ln(J/E_{ox}^2)$ vs. $(1/E_{ox})$, as shown in Figure 6. The slope of this curve in the F-N tunneling regime is measured which is given by[18]

$$S = \frac{d\left[\ln\left(\frac{J}{E_{ox}^2}\right)\right]}{d\left(\frac{1}{E_{ox}}\right)} = -\frac{8\pi\sqrt{2m_{ox}}}{3hq}(\Delta E_c)^{\frac{3}{2}} = const.$$
$$= -3.1488 \times 10^{10}.$$

Using the calculated slope (S) and assuming an electron effective mass of SiO_2 is $0.4m_0$,[29,30] the ΔE_C was calculated to be 3.76 eV, which is close to the result obtained from XPS. Taking bandgap of SiO_2 and Ga_2O_3, band offset

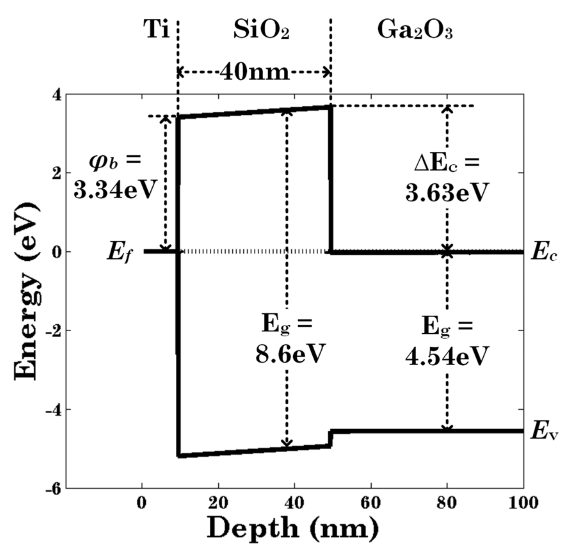

FIG. 7. Calculated band diagram of MOSCAP device at zero bias. The bandgap and conduction band offset were extracted by XPS. Both I-V characteristics and XPS show similar conduction band offset, ~3.7 eV.

obtained from XPS, doping density as $9 \times 10^{18}/cm^3$, barrier height between Ti and SiO_2 as 3.34 eV, a calculated band diagram at zero bias is shown in Figure 7.

In summary, we evaluated the band alignment between ALD SiO_2 and *n*-doped β-Ga_2O_3 $(\bar{2}01)$ by XPS and electrical measurements. The conduction band offset is determined to be 3.63 and 3.76 eV by XPS and electrical measurements, respectively. The large conduction band offset is useful for power devices, especially for high temperature operation. However, the dielectric constant of SiO_2 is lower than Al_2O_3, which reduces the equivalent oxide thickness (EOT). A composite gate dielectric stack with thin interfacial SiO_2 layer and thicker Al_2O_3 layer can be used to obtain both large conduction band offset and lower EOT.

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