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Enhancement-Mode N-Polar GaN Metal–Insulator–Semiconductor Field Effect Transistors with Current Gain Cutoff Frequency of 120 GHz

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We report the small-signal high-frequency performance of novel enhancement-mode N-polar GaN metal–insulator–semiconductor field effect transistors with a peak short-circuit current gain cutoff frequency (f_t) of 120 GHz for a 70-nm gate length device. The device has an 8-nm GaN channel with AlN back barrier and a 5-nm SiN_x gate dielectric. These devices show a peak drain current of 0.74 A/mm and peak transconductance of 260 mS/mm at a drain bias of 3.0 V. This is the first demonstration of high-frequency operation of N-polar enhancement-mode GaN devices.

There has been increased interest in high-performance enhancement-mode (E-mode) GaN field effect transistors (FETs) for high-frequency, and high-breakdown applications. E-mode devices with good DC characteristics, high short-circuit current gain cutoff frequency (f_t) (~112 GHz), and high power gain cutoff frequency (f_{max}) (~215 GHz)[1–6] have been demonstrated. Recently, promising alternative GaN technologies such as InAlN top-barrier,[7] and InGaN back-barrier devices[8] are being investigated to extend the high-frequency operation of GaN devices. N-polar GaN technology, with potential advantages in the carrier confinement in the channel is one such novel technology that is being explored.[9–11] Self-aligned N-polar GaN technology with degenerately doped n^+ source/drain regions would reduce the source access resistance. Depletion mode (D-mode) N-polar GaN FETs with self-aligned source/drain, and with a f_t of 132 GHz, at a gate length (L_g) of 120 nm have been demonstrated.[9] We recently reported self-aligned N-polar E-mode GaN metal–insulator–semiconductor FETs (MISFETs) with n^+ source/drain regrowth, and with a 20-nm GaN channel; where the E-mode operation was obtained through the polarization field of a top-AlN electron depleting layer. These devices show a high drain current (I_d) of 0.74 A/mm and an extrinsic f_t of 18 GHz.[12] However, the devices become D-mode at $L_g = 0.18\,\mu m$ due to threshold voltage (V_{th}) roll off. In order to obtain high-frequency E-mode operation of the N-polar GaN devices at sub-100-nm gate lengths, the vertical dimensions of the device have to be scaled. In this letter, we report the high-frequency performance of self-aligned E-mode N-polar GaN FETs obtained by simultaneous vertical and lateral scaling of the device, enabling E-mode operation for $L_g = 70$ nm. These devices show a peak I_d of 0.74 A/mm and peak transconductance (g_m) of 260 mS/mm. A peak f_t of 120 GHz was obtained for the $L_g = 70$ nm device.

The cross-section schematic and layer structure of the self-aligned device is shown in Fig. 1, where the device structure was vertically scaled by reducing the GaN channel thickness from the previously reported self-aligned N-polar E-mode devices.[12] Devices with an 8-nm GaN channel, with-2 nm AlN back-barrier, and a 2 nm top AlN layer (Fig. 1) were grown by plasma-assisted molecular beam epitaxy (PA-MBE) on a C-face SiC substrate.[13] E-mode operation of the device is enabled by the polarization induced field of the 2-nm AlN capping layer, which depletes the two-dimensional electron gas (2DEG) [Fig. 1(b)]. Removal of the AlN layer from the access regions recovers the 2DEG [Fig. 1(c)] under both the sidewall access and the source access regions. Hall measurement of the as-grown wafer and one with 5-nm SiN_x deposited by high-temperature chemical vapor deposition (HT-CVD) did not show any mobile charge. The measured 2DEG density after AlN removal and deposition of 40 nm of plasma-enhanced CVD (PE-CVD) SiN_x is $7.5 \times 10^{12}\,cm^{-2}$, which matches with the simulated 2DEG density as shown in Fig. 1(c).

A refractory gate-stack, W (50 nm)/Cr (50 nm)/SiN_x (300 nm), with 5-nm of HT-CVD SiN_x gate dielectric was fabricated following the process in ref. 12 with a gate length of 70 nm defined by electron beam lithography. After 40 nm of PECVD SiN_x sidewall formation, a graded n^+ InGaN (40 nm)/InN (10 nm) contact layer was regrown by PA-MBE to reduce the access and contact resistances.[14]

The common source input and output characteristics of the device in Fig. 2 show E-mode operation. Unlike the previously reported devices in ref. 12, E-mode operation is maintained at a gate length of 70 nm for the 8-nm GaN channel device because of the vertical scaling. The threshold voltage is 0.7 V at a drain bias (V_{ds}) of 3.0 V, which was extracted by the linear extrapolation of I_d–gate voltage (V_{gs}) plot to zero drain currents. The device shows a V_{th} which decreases with increasing drain bias because of drain-induced-barrier-lowering (DIBL). The peak I_d and peak g_m are 0.74 A/mm and 260 mS/mm, respectively at a drain bias of 3.0 V. The three terminal breakdown voltage is 12 V at a gate bias of 0 V.

Small-signal characterization of the device from 250 MHz to 67 GHz was carried out on an Agilent E8361A network analyzer. First, an off-wafer probe tip calibration on a standard substrate was carried out. Next, on-wafer open-short calibration standards were used to de-embed the pad parasitics[15] and to extract the intrinsic device cut-off frequency. Figure 3(a) shows the short-circuit current gain (h_{21}) after pad de-embedding for the 70-nm gate length device at $V_{gs} = 2.5$ V and $V_{ds} = 3.0$ V, from which a f_t of 120 GHz is extrapolated. To the best of our knowledge this is the highest reported f_t for E-mode GaN devices. Figures 3(b) and 3(c) show the variation of current gain cutoff frequency with gate bias and drain bias, respectively.

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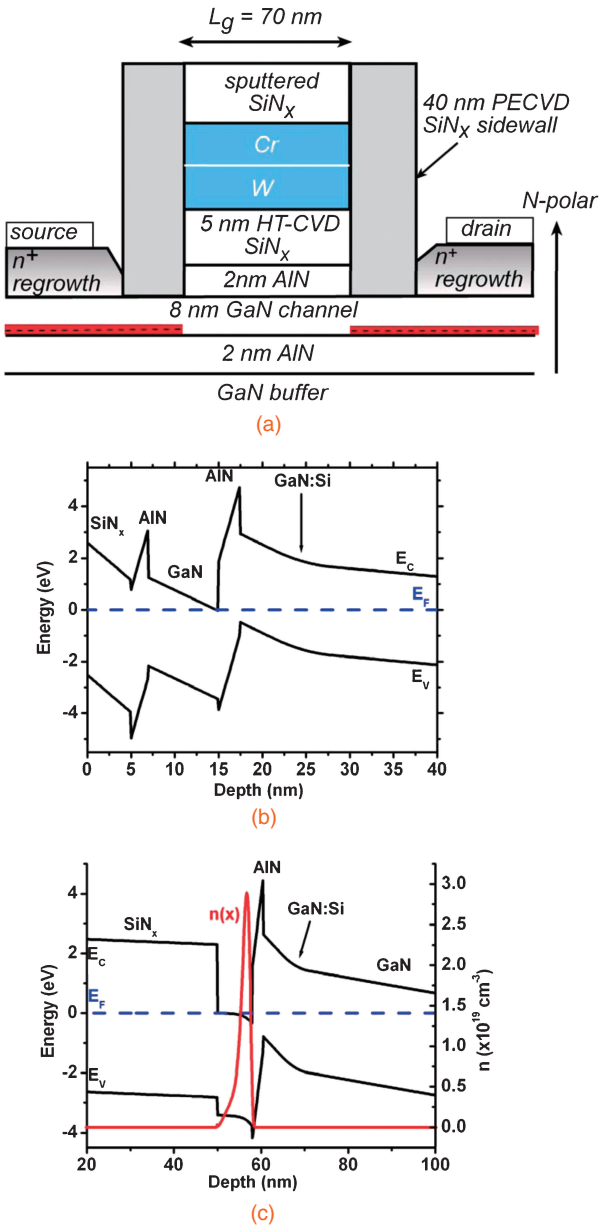

Fig. 1. (a) Device cross-section schematic. (b) Band diagram under the gate showing E-mode operation. (c) Band diagram under the SiN_x sidewall access region.

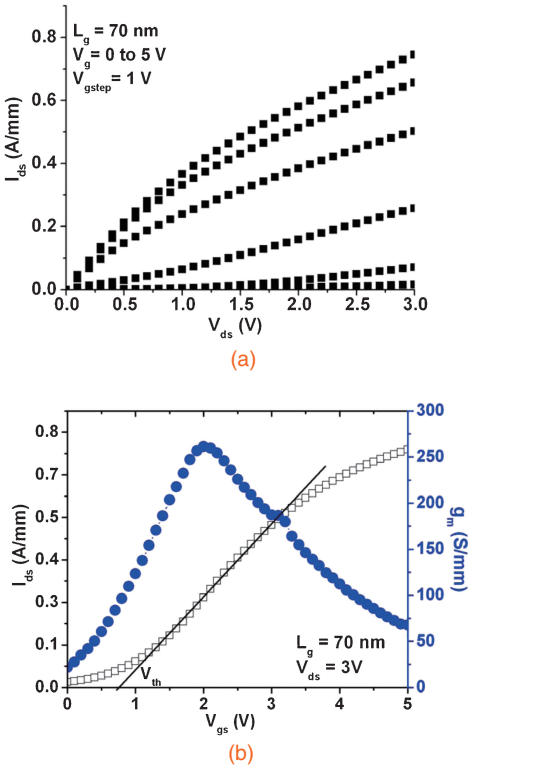

Fig. 2. Common-source output and input characteristics of the 70 nm gate length device.

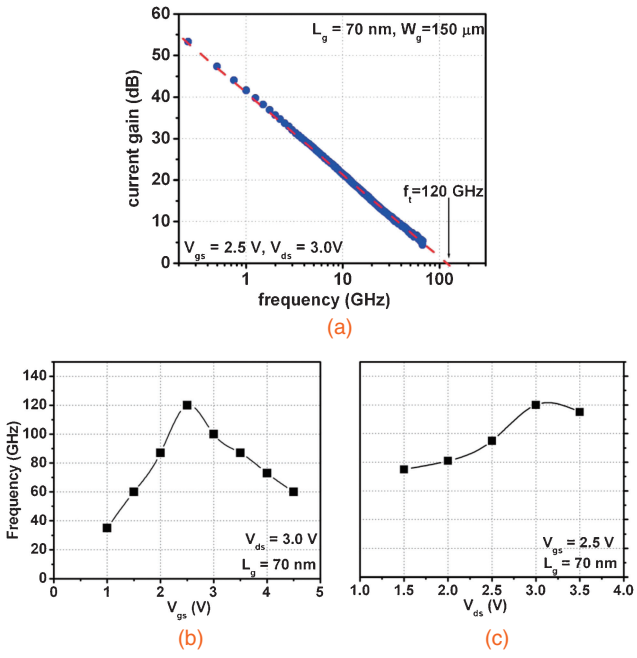

Fig. 3. (a) Measured short circuit current gain (h_{21}) vs frequency of the device. A current gain cut off frequency (f_t) of 120 GHz is extrapolated. (b) f_t versus gate voltage for $V_{ds} = 3.0$ V, and (c) f_t versus drain bias for $V_{gs} = 2.5$ V.

The peak f_t occurred at $V_{gs} = 2.5$ V, while the peak in g_m occurred at $V_{gs} = 1.75$ V. The difference in the V_{gs} for peak g_m and peak f_t could be due to a possible difference in the gate-to-drain capacitance (C_{gd}) at different gate biases. The f_t increases with increasing drain bias at a given V_{gs} because of the increase in the transconductance with increasing V_{ds}, which is seen in the DC output characteristics. The f_{max} of the device was 11 GHz at $V_{gs} = 2.5$ V and $V_{ds} = 3.0$ V, which is low due to the high gate resistance of the thin W gate. Such high f_t and low f_{max} performance was also observed in the previously reported thin W gate devices.[9] Incorporation of the top T-gate process[16] would reduce the gate resistance resulting in high f_t and f_{max} simultaneously.

Although the devices show high f_t, the DC output characteristics show poor saturation and high output conductance, both of which are critical parameters for analog circuits. We ascribe the observed high output conductance to the possible presence of positively charged traps at the bottom-AlN/GaN-buffer interface (negative polarization interface) below the channel. It has been observed that the output conductance of N-polar devices depends on the back-

barrier design.[17] The physical origin of the dependence of output conductance on the back-barrier design is currently under investigation and will be reported in a different publication. The output conductance due to the back-barrier is further enhanced in the present devices because of the self-aligned drain and low gate-length to gate-to-2DEG aspect ratio. This aspect ratio for the reported device is 4.6 at which short-channel effects are known to be severe.[18,19] The n^+ self-aligned drain further increases the output conductance. This is due to a lower voltage drop in the access region leading to a higher voltage at the drain edge of the transistors. Such enhanced two-dimensional (2D) electrostatic effects have also been reported in non-lightly-doped-drain metal–oxide–semiconductor FETs (non-LDD-MOSFETs). This effect is present in the non-LDD-MOSFETs because of the lower voltage drop in the drain access region compared to the case of LDD-MOSFETs.[20]

The on-resistance (R_{on}) of the device is 2.6 Ω mm, which is higher than the previously reported R_{on} of the self-aligned E-mode devices.[12] The higher R_{on} could be ascribed to the highly resistive regrowth due to un-optimized growth conditions compared to the previously reported MISFETs.[12] Optimized regrowth conditions will improve the R_{on} of the device. Besides the regrowth sheet resistance, the sidewall access resistance is also high on these devices. Hall measurement on process monitor wafers with 40 nm of PE-CVD SiN_x shows a sheet resistance of 2370 Ω/□ with a 2DEG density of $7.5 \times 10^{12}\,cm^{-2}$ and a mobility of $350\,cm^2\,V^{-1}\,s^{-1}$. Higher surface scattering could be the reason for the observed low mobility in the sidewall access regions. Reduction of surface scattering and thinner sidewalls will decrease the contribution of the sidewall regions to the source access resistance.

In conclusion, we have demonstrated E-mode N-polar GaN MISFET devices with an 8-nm GaN channel, and with a highest f_t of 120 GHz at a gate length of 70 nm. The future devices have to be optimized for low output conductance by further vertical scaling of the channel and the gate dielectric, and also by the optimization of the back barrier design. The growth and structures will also have to be optimized to reduce surface scattering in order to maintain high mobility in the sidewall access regions.

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