CMOS compatible integrated ferroelectric tunnel junctions (FTJ)

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Outline

• Introduction and motivation

• Background and previous work

• Integrated FTJ device process

• Device results and discussion

• Conclusion
Motivation

Evolution of Extended CMOS

Functional scaling of CMOS
- More Than Moore elements
- Beyond CMOS devices
- Non-charge based devices for beyond CMOS

ITRS Roadmap, Emerging Research Devices (ERD), (2011)
Beyond CMOS devices

- Exploit novel materials properties: spin, magnetic, ferroelectric
- Devices based on ferroelectrics: FE memory, FE FET, FE FTJ
- FE based devices for memory, logic, logic in memory
Ferroelectric tunnel junctions (FTJs)


Ferroelectric tunnel junction (FTJ) devices

- Tunnel current modulated by the polarization of FE material
- Large ON/OFF ratio
- Non-volatile state $\rightarrow$ novel FTJ based circuits
FTJ vs FeRAM

FTJ advantages:

• Non-destructive readout: based on measuring the tunneling conductance
• Good scalability: tunnel current can be measured for deep sub-\(\mu m\) junction
• Low read power: read voltage below \(V_c\)
Non-integrated FTJs


Non-integrated device using AFM tip as an electrode

- Quick and fast technique to test device structures
- Hard to test scalability and CMOS compatibility
- Hard to do high speed switching tests

FTJ Integration required?
$n$-LSMO(30nm)-BTO(1.6nm)-Co(5nm) FTJ simulation:

- FE barrier height ($\phi_b$) changes from $P\uparrow$ to $P\downarrow$.
- Effective tunnel barrier width ($t_b$) changes from $P\uparrow$ to $P\downarrow$.
- Transmission probability modulated.

Electronic parameters of LSMO, BTO and Co used are:
- $E_{g_{LSMO}}=1$ eV, $E_{g_{BTO}}=3.3$ eV, $\chi_{LSMO}=4.8$ eV, $\chi_{BTO}=2.5$ eV, $\phi_{CO} = 5$eV.
- $n^+=5\times10^{19}$/cm$^3$.

Energy band diagram of LSMO(30nm)-BTO(1.6nm)-Co(5nm) FTJ. $P=\pm 40\mu C/cm^2$.
Scalable FTJ process flow

1) As grown sample with blanket Co/Au

2) Lift-off Ti/Au/Ni anode contact

3) Self aligned RIE etch of Co/Au/BTO with Ni etch mask

4) Cathode contact (Ti/ Au) lift-off

5) RIE etch n⁺ LSMO

6) Sidewall process using ALD HfO2

7) Lift-off anode contact pad on insulating NGO

Layout of 3×3μm² area FTJ diode with RF contact pad

Device Research Conference, June 21-24, 2015, Ohio State University
FTJ Fabrication

- FTJs fabricated with 4 unit cells of BTO
- Minimum device area 3 \( \mu \text{m} \times 3 \mu \text{m} 
- Process yield is good
- Devices show switching behavior
• Switching observed in 3 µm X 3 µm to 7 µm X 7 µm diodes
• Read voltage ±0.2V, write voltage ±0.6V~Low power operation

FTJ Switching

Anode PAD

Etched LSMO

~200nm separation

Cathode PAD

FTJ anode

V_{write} = ±0.6V

Read Voltage (V)

Current (µA)

3 µm X 3 µm FTJ I-V

300

200

100

0

-100

-200

-300

-0.2

-0.1

0

0.1

0.2

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FTJ Switching

Peak $I_{on}/I_{off} = 60$ observed in a $5 \, \mu m \times 5 \, \mu m$ device

Resistance loop is the fingerprint of FE polarization reversal

Device switching yield is very poor ( < 10 %)
FTJ device yield

- Devices that show switching were misaligned

- Devices with good alignment show insulating behavior
Non switching FTJs

- Good lithography alignment
- Minimum access length >5\(\mu\)m along X & Y-direction
- Large parasitic resistance (>T\(\Omega\)) on LSMO along X & Y-direction
- Applied voltage dropped across insulating LSMO
• High resistance observed on LSMO layer
• Bad contact with Ti/LSMO
• Damage due to RIE
FTJ device yield

- High resistance observed on LSMO layer
- Misaligned device $\rightarrow$ reduced resistance $\rightarrow$ FTJ switching
- Devices with good alignment $\rightarrow$ high resistance
After RIE and O₂ plasma

- Pt/Au, Ag, and Ti/Au TLM structure on bare LSMO
- All the metal layers show good ohmic behavior
- LSMO layer exposed to RIE process
- Ti contacts after RIE/O₂ plasma show high resistance
- SRO electrode instead of LSMO

Bare LSMO

After RIE and O₂ plasma
Sub-micron FTJ

Sum-micron FTJ without contact PAD

- Sub-micron anodes fabricated by electron beam lithography
- FTJ characteristics measured by AFM
- Devices show polarization loop
Conclusion and future work

- Integrated FTJ process demonstrated
- FTJ switching in integrated process
- Sub-micron dimension FTJ processed
- Contact degradation of etched LSMO layer
- Need FTJ electrode $\rightarrow$ SRO
- Integrate FTJ with SRO electrode future
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