Temperature dependent quasi-static capacitance-voltage characterization of SiO_2/β–Ga_2O_3 interface on different crystal orientations

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Citation: Appl. Phys. Lett. **111**, 122108 (2017); doi: 10.1063/1.4991400
View online: http://dx.doi.org/10.1063/1.4991400
View Table of Contents: http://aip.scitation.org/toc/apl/111/12
Published by the American Institute of Physics

Temperature dependent quasi-static capacitance-voltage characterization of SiO_2/β-Ga_2O_3 interface on different crystal orientations

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(Received 20 June 2017; accepted 12 September 2017; published online 21 September 2017)

The interface trap density (D_{it}) of the SiO_2/β-Ga_2O_3 interface in ($\bar{2}01$), (010), and (001) orientations is obtained by the Hi-Lo method with the low frequency capacitance measured using the Quasi-Static Capacitance-Voltage (QSCV) technique. QSCV measurements are carried out at higher temperatures to increase the measured energy range of D_{it} in the bandgap. At room temperature, higher D_{it} is observed near the band edge for all three orientations. The measurement at higher temperatures led to an annealing effect that reduced the D_{it} value for all samples. Comparison with the conductance method and frequency dispersion of the capacitance suggests that the traps at the band edge are slow traps which respond to low frequency signals. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4991400]

Gallium Oxide (Ga_2O_3) power device research has been experiencing a rapid growth in recent years due to its many attractive merits. It has been reported that β-Ga_2O_3, its most stable form, has higher Baliga's Figure of Merit (BFoM) than GaN and SiC,[1] making it an attractive material for power devices. In addition to its promising material properties, growth techniques are well developed and are used to manufacture high quality substrates with controllable doping density, which are also commercially available.[2–5] This will not only lower the cost of β-Ga_2O_3 power devices but also make them more competitive and give rise to a fast market adoption. Many experimental breakthroughs have been demonstrated including depletion[6–8] and enhancement-mode[9–11] metal oxide semiconductor field effect transistors (MOSFETs), record high drain current densities,[12] and high operational fields[13] in MOSFETs, 1-kV Schottky diodes,[14] field-plated high-breakdown MOSFET,[15] and Radio Frequency (RF) MOSFET.[16] All these results at an early stage of Ga_2O_3 research show the immense potential of β-Ga_2O_3 for power devices.

Although many devices have been successfully demonstrated, there is a limited report on the dielectric interface properties of β-Ga_2O_3.[17,18] The interface properties play an important role in the operation of metal oxide semiconductor field effect transistors (MOSFETs). Interface traps impact the gate voltage modulation, thus affecting the subthreshold slope, threshold voltage, and output current. Therefore, it is important to quantify the density of interface traps (D_{it}) at the dielectric-Ga_2O_3 interface for a better understanding of device operation and also to guide the design of MOSFETs. In addition, several different crystal orientations have been used in previously published device and growth reports.[12,15,16] The crystal orientation has been shown to impact the growth rates.[19] At this early stage of development, there is interest in exploring different crystal orientations for devices. Therefore, it is also necessary to understand the impact of the crystal orientation on the dielectric interface properties.

In this letter, we report the D_{it} value at SiO_2/β-Ga_2O_3 interfaces in ($\bar{2}01$), (010), and (001) crystal orientations by using temperature dependent Quasi-Static Capacitance-Voltage (QSCV) and high frequency (HF) C-V measurements on MOS capacitors (MOSCAPs).[20] This technique of extracting D_{it} covers a wider energy range in the bandgap than the conductance method. It also probes very slow responding states, which are not probed in the conductance method. These slow interface traps may have an impact on the device operation under certain conditions.[21,22] The D_{it} value is extracted using the Hi-Lo method proposed by M. Kuhn,[23] where the difference between high frequency (Hi or HF) capacitance and low frequency (Lo or QSCV) capacitance at each gate bias determines the D_{it} value at that gate bias, which is given by

$$D_{it}(V_g) = \left(\frac{C_{OX}C_{Lo}}{C_{OX}-C_{Lo}} - \frac{C_{OX}C_{Hi}}{C_{OX}-C_{Hi}}\right)\Big/ qA, \qquad (1)$$

where C_{OX} is the oxide capacitance measured at accumulation, C_{Lo}, and C_{Hi} are the QSCV and HFCV capacitances at the corresponding gate bias, q is the electronic charge, and A is the effective gate area. The gate bias (V_g) is then translated into the distance from the conduction band edge (ΔE) by comparing the HFCV curve with a surface potential (ϕ_s) vs. ideal HF capacitance (C_{ideal}) curve generated by calculating the exact solution for MOS electrostatics.[24] This calculation assumes that at a certain gate bias, C_{Hi} and C_{Lo} are measured at the same ϕ_s value. At a given ϕ_s value, regardless of surface properties, HF capacitance should be constant. For the ideal HFCV calculation of SiO_2/β-Ga_2O_3 MOSCAP, the relative permittivity of Ga_2O_3 is assumed to be 10 and its electron effective mass ratio is 0.28 which is isotropic near the conduction band minima.[1,25–27] This calculation gives a D_{it} vs. ΔE curve.[28] However, the valid range of energies (ΔE) for quantitative D_{it} extraction is reduced, which is limited by the temperature, the high frequency, and the low frequency (QSCV)[20] of the measurement. This range is determined by the Shockley–Read–Hall statistics of capture and emission rates that govern the dynamics of interface traps

$$\tau = \frac{\exp\left(\frac{\Delta E}{kT}\right)}{\sigma v_t N}, \qquad (2)$$

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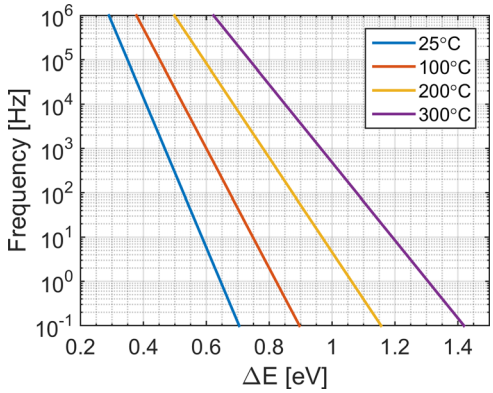

FIG. 1. Trap frequency vs. its energy level from the conduction band edge (ΔE) at room temperature, 100 °C, 200 °C, and 300 °C plotted for β-Ga_2O_3. The frequency range and temperatures shown in the plot are used in the experiment.

where $\tau = 1/f$, f is the frequency in Hz, k is the Boltzmann constant, T is the temperature, σ is the capture cross-section of the trap that is assumed to be 1×10^{-15} cm^2, v_t is the average thermal velocity of electrons, and N is the effective density of states in the conduction band. This equation is plotted for β-Ga_2O_3 at room temperature (RT), 100 °C, 200 °C, and 300 °C in Fig. 1. As shown in Fig. 1, at room temperature for a HF frequency of 1 MHz and a QSCV frequency of 0.1 Hz, only a small ΔE from 0.3 eV to 0.7 eV is probed. Thus, the D_{it} value extracted using this technique at RT is not valid outside this energy range. Therefore, QSCV measurements at elevated temperatures are necessary to probe any interface states deeper than 0.7 eV.

For the MOSCAP fabrication, three β-Ga_2O_3 substrates with ($\bar{2}01$), (010), and (001) surface orientations are used to study the dependence of D_{it} on crystal orientation. The substrates were grown by Tamura Corporation with an unintentionally n-type doping (UID) density in the range of 2×10^{17}/cm^3 to 5×10^{17}/cm^3. First, all samples were cleaned using the standard solvent clean procedure. Then, a blanket layer of 70 nm of SiO_2 was deposited at 300 °C on all samples simultaneously in an Oxford FlexAL atomic layer deposition (ALD) tool using the Tris(dimethylamino)silane (3DMAS) precursor and O_2 plasma. To form an ohmic contact, the oxide in the contact region is etched away by CF_4/O_2 based reactive ion etching (RIE). Next, the Ti(20 nm)/Al(100 nm)/Ni(50 nm)/Au(50 nm)[13] contact is deposited followed by a 470 °C 1 min and 600 °C 1 min annealing sequence in a rapid thermal anneal (RTA) oven under a nitrogen gas flow. Two-step annealing is required to achieve a low enough contact resistance at the given doping density. It is necessary to reduce the ohmic resistance so that a low dissipation factor is obtained for HF capacitance measurements. Otherwise, when the dissipation factor is high, the measured HF capacitance $C_{m,Hi}$ will deviate significantly from the true C_{Hi},[29] which will introduce large error in the obtained D_{it} value. At last, the Ti/Au gate electrodes were re-aligned to the MOSCAP by standard photolithography and deposited using an electron-beam evaporator.

The QSCV measurement is carried out using a Keithley 595 quasistatic CV meter in the square-wave mode.[20,30] In this mode, at a given gate bias, a small voltage step (100 mV) is applied and then turned off repeatedly, generating a square wave. The delay time is set to 2 s, with a duty ratio of 50%, and thus, the period is 4 s, making the effective measurement frequency 0.25 Hz. The charge displacement current due to the voltage step up is measured by the feedback charge method right before the voltage step down. The measurement is repeated 12 times at each gate bias and averaged to reduce the noise. After this bias, the gate voltage is reset to the next value and the process continues until all the required gate bias points have been measured. This measurement results in a voltage ramp rate of 1 V/min. The entire QSCV measurement is automated by a custom LABVIEW program. Immediately after the QSCV measurement, a 1 MHz HFCV is measured using an Agilent 4294A precision impedance analyzer and a 42941A impedance probe at the same bias points and the same sweep direction. The measured Hi and Lo capacitances on three samples at room temperature are shown in Fig. 2(a), and the corresponding D_{it} obtained using Hi-Lo analysis is shown in Fig. 2(b). It can be seen in Fig. 2(b) that the ($\bar{2}01$) sample has the highest D_{it} value, while (001) has an intermediate and (010) has the lowest D_{it} value for energies higher than 0.3 eV ($\Delta E > 0.3$ eV). In addition, the profile of the D_{it} values in that energy range is different for ($\bar{2}01$) as compared to the other samples. However, the D_{it} value near the band edge is the same for all the samples. In Fig. 2(b), two capacitors are measured for each sample to measure any local variation in the samples. Although a local variation is observed, the figure clearly shows the difference in D_{it} due to the crystal orientations. The observed difference in D_{it} between different samples could be due to the difference in the initial bonding configuration between SiO_2 and Ga_2O_3 in different crystal orientations. Further comprehensive advanced analytical studies

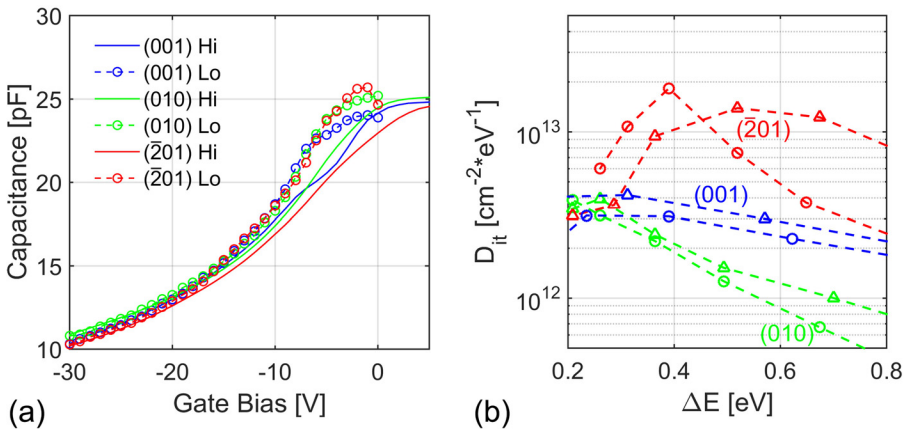

FIG. 2. (a) Hi-Lo CV curves measured on three samples at room temperature, on 200 μm × 225 μm MOSCAPs. (b) Obtained D_{it} from the Hi-Lo curves in (a); the energy range is limited from 0.2 to 0.8 eV at room temperature according to Fig. 1. Two D_{it} curves obtained on each sample show the local variation of D_{it}.

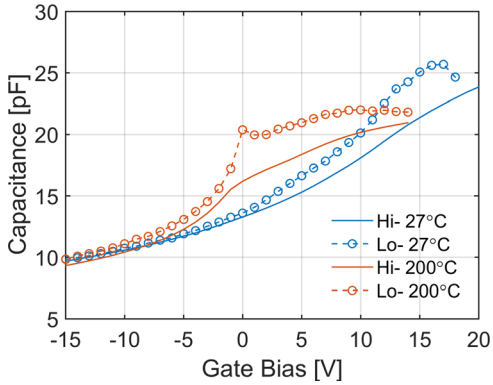

FIG. 3. Comparison of measured Hi-Lo CV curves between room temperature and 200 °C for the ($\bar{2}$01) sample (200 μm × 225 μm MOSCAP). Gate bias is corrected for flat-band voltage shifts to present a comparative view.

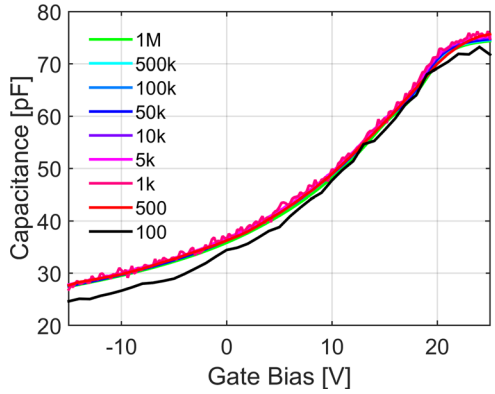

FIG. 5. Frequency dispersion of the CV characteristic of (001) sample MOSCAP (300 μm × 450 μm) at room temperature. Minimum dispersion is observed down to 500 Hz. The 100 Hz deviation is most likely due to the border traps or leaky layer adjacent to the interface[36] since interface traps only increase capacitance.

are necessary to identify the origin of the differences.[31–33] It is noted that the ($\bar{2}$01) sample shows much higher D_{it} than our previously reported data.[17] This is attributed to the additional 600 °C 1 min ohmic contact annealing that was not present in the previously reported sample. In addition, the difference also arises from the slow traps, which are probed in QSCV but not in the conductance method which was used in the previous report.[17]

Furthermore, in order to increase the range of energies probed for D_{it}, QSCV and HFCV were measured at elevated temperatures for all the samples. Figure 3 shows the comparison of Hi-Lo CV curves at room temperature and 200 °C for the ($\bar{2}$01) sample. The horizontal stretch-out observed in the HFCV at 200 °C is from −2 to 14 V, producing a signature ledge that is observed on all samples. This stretch-out is due to the DC filling of D_{it}. The kink seen at zero bias in the QSCV curve at 200 °C is due to the lateral charge motion when switching bias polarity.[20] Similar QSCV curves (see supplementary material) are observed for all the three samples at higher temperatures including the ledge and the kink at zero bias.

The obtained D_{it} value from the Hi-Lo method at different temperatures is shown in Fig. 4 for all three samples. From Figs. 4(a)–4(c), it can be seen that all three samples show a decrease in D_{it} in band edge states at elevated temperatures (≥200 °C) and the range of probed energies is also increased. It is also interesting to note that one temperature as shown in Fig. 1 can access energy levels overlapping with another temperature. Because of this feature, it is possible to

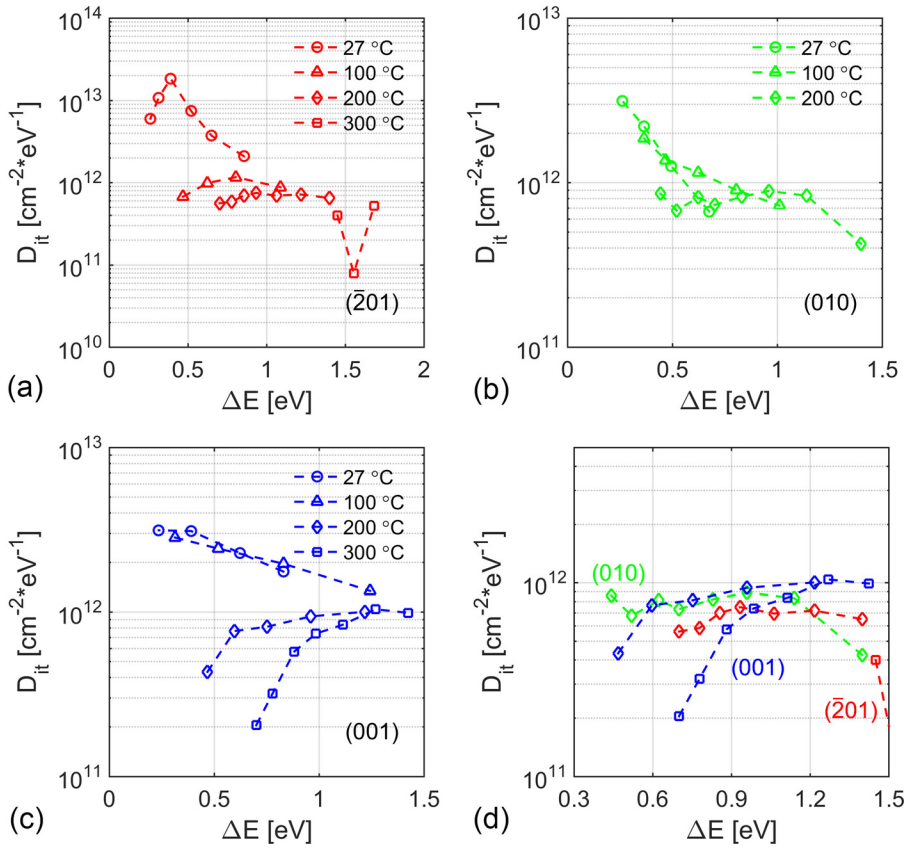

FIG. 4. D_{it} vs. ΔE obtained from the Hi-Lo method at different temperatures for (a) (201) sample, (b) (010) sample, and (c) (001) sample. The energy range displayed at each temperature is limited according to Fig. 1. (d) shows D_{it} from high temperature measurements (≥200 °C) for all three samples. 300 °C data on the (010) sample are not measured due to high gate leakage.

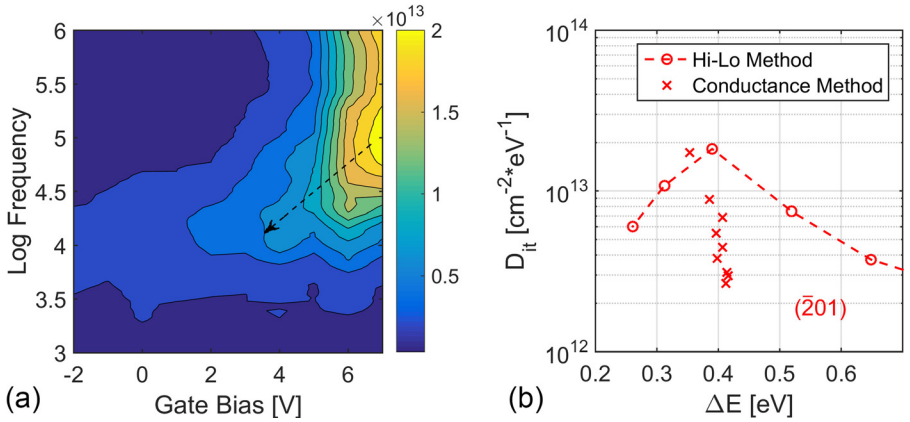

FIG. 6. (a) Color map of D_{it} values from the conductance method, as a function of gate bias and frequency, measured at room temperature for the ($\bar{2}$01) sample. The arrow shows the movement of the peak in response to gate bias. (b) Comparison of D_{it} obtained using the Hi-Lo method and the conductance method.

probe D_{it} at the same energy level repeatedly at different temperatures. Figure 4(d) shows the D_{it} value from all the samples measured at higher temperatures ($\geq 200\,^{\circ}$C). It can be seen that the D_{it} value is lower than 1×10^{12}/cm^2·eV for all the samples at higher temperature measurements. As the QSCV measurement takes few hours, the high temperature measurements in fact anneals the dielectric interface and reduces the D_{it}. Thus, at higher temperature, at the same energy level, the obtained D_{it} value becomes lower. Most change can be observed in the ($\bar{2}$01) sample since it has the highest D_{it} value at the band-edge at room temperature, which is mostly attributed to slow traps as explained later. For the (010) sample, only a small decrease is observed at higher temperature since the slow trap density is already low at room temperature. It is observed that after 200 °C measurements and concurrent anneal, most slow traps are suppressed and all three samples have very similar D_{it} of $< 1 \times 10^{12}$/cm^2·eV [Fig. 4(d)] in the probed energy range. After the high temperature measurement, the D_{it} value was again measured at room temperature (see supplementary material), which gave a reduced D_{it} value clearly indicating the annealing effect of the high temperature measurements. The reduction in D_{it} due to the annealing effect could be attributed to the reduction in dangling bonds at the interface.[34]

The high density of D_{it} at room temperature near the band-edge is attributed to slow traps. This is verified from the capacitance frequency dispersion and conductance method. Figure 5 shows the capacitance frequency dispersion of the (001) sample at room temperature, and similar curves (see supplementary material) are observed for the other two samples. Compared to Fig. 2(a) Hi-Lo CV, no significant increase in capacitance is observed near the accumulation region in Fig. 5 for the lowest frequency. This suggests that a majority of D_{it} values obtained in Fig. 2(b) are below 100 Hz and above 0.25 Hz and thus slow traps. These slow traps also have large time constant dispersion, smearing out the QSCV profile in the corresponding regions.[35] Figure 6 shows a conductance method measurement at room temperature for ($\bar{2}$01) orientation as an representative example. In Fig. 6(b), the conductance method clearly shows lower D_{it} at the band-edge compared to the Hi-Lo method as it only covers frequencies from 1 kHz to 1 MHz, which exclude all the slow traps. Future optimization should be focused on minimizing these slow traps at the band-edge as well as fast traps over all the energy levels.

In summary, we obtained the D_{it} value at SiO_2/β-Ga_2O_3 interfaces for ($\bar{2}$01), (010), and (001) crystal orientations by using the temperature dependent QSCV technique. At room temperature, the ($\bar{2}$01) sample showed the highest D_{it} value, which is attributed to slow traps by comparing with frequency dispersion. Higher temperature measurements increased the range of D_{it} values probed. The long measurement times at higher temperatures show an annealing effect and reduce the D_{it} value for all samples. After thermal annealing during the long temperature dependent measurements, the D_{it} value for all samples decreases to a similar average value of $\sim 6 \times 10^{11}$/cm^2·eV between 0.45 and 1.5 eV below the conduction band edge.

See supplementary material for the comparison of the QSCV curves and frequency dispersion of all three samples and the measured D_{it} value at room temperature after high temperature measurements.

This work was supported by the National Science Foundation (NSF) Grant (ECCS 1607833) monitored by Dr. Dimitris Pavilidis. A portion of this work was performed in University at Buffalo, Davis Hall Electrical Engineering Cleanroom. The authors would like to thank the support from cleanroom staff.

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