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ARTICLE

Gate-Controlled Metal−Insulator Transition in TiS_3 Nanowire Field-Effect Transistors

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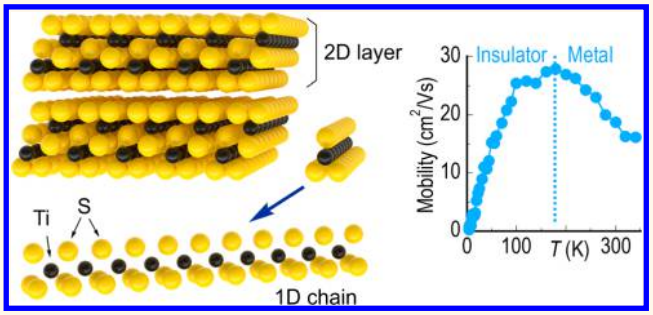
Supporting Information

ABSTRACT: We explore the electrical characteristics of TiS_3 nanowire field-effect transistor (FETs), over the wide temperature range from 3 to 350 K. These nanomaterials have a quasi-one-dimensional (1D) crystal structure and exhibit a gate-controlled metal−insulator transition (MIT) in their transfer curves. Their room-temperature mobility is ∼20−30 $cm^2/(V\ s)$, 2 orders of magnitude smaller than predicted previously, a result that we explain quantitatively in terms of the influence of polar-optical phonon scattering in these materials. In the insulating state (<∼220 K), the transfer curves exhibit unusual mesoscopic fluctuations and a current suppression near zero bias that is common to charge-density wave (CDW) systems. The fluctuations have a nonmonotonic temperature dependence and wash out at a temperature close to that of the bulk MIT, suggesting they may be a feature of quantum interference in the CDW state. Overall, our results demonstrate that quasi-1D TiS_3 nanostructures represent a viable candidate for FET realization and that their functionality is influenced by complex phenomena.



KEYWORDS: *titanium trisulfide, transition-metal trichalcogenides, metal−insulator transition,, charge-density wave, one-dimensional nanostructures*

As the scaling of transistors approaches the atomic realm, there has been enormous interest in the possibility of utilizing two-dimensional (2D) materials as potential channel replacements for silicon.[1] The ultrathin nature of these materials renders them immune to many short-channel effects[2] and allows them to exhibit large subthreshold slope.[2] They also allow the prospect of devices with enhanced functionality, such as multivalued logic and low-power spintronic transistors.[3] Among the different materials that have been explored to date, much interest has focused on the transition-metal dichalcogenides[4,5] (TMDs), with general chemical formula MX_2 (where M is a transition metal such as Mo or W and X is a chalcogen). The large bandgap (>1.5 eV) of these materials allows the realization of field-effect transistors (FETs) with ON/OFF ratios of $>10^8$, while the direct band structure of their monolayers enables numerous optoelectronic opportunities.[6−11] Closely related to the TMDs are the transition-metal trichalcogenides[12−14] (TMTs), with general chemical formula MX_3. While the properties of these materials have been less widely studied than those of TMDs, especially in few-layer form, there are a number of indications that they could also provide excellent channel replacements. In this Article, we focus specifically on an analysis of the characteristics of FETs implemented from TiS_3, a group IV TMT in which the full structure of the crystal may be viewed as comprising an interconnected array of one-dimensional

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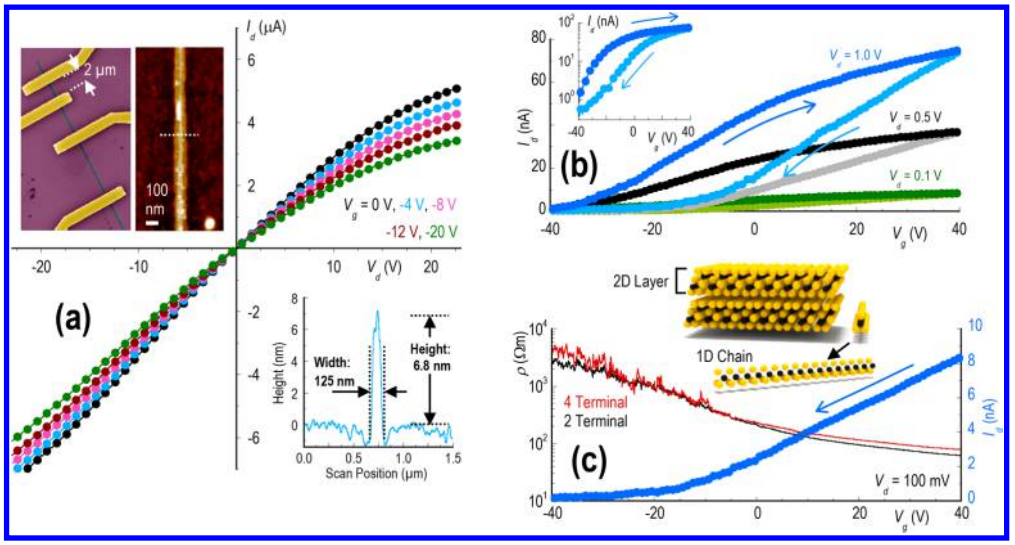

Figure 1. The various panels indicate the results of room-temperature characterization of the TiS_3 nanowire FETs. (a) The main panel plots two-terminal transistor curves of D1 at various gate voltages (indicated). In the upper-left quadrant of the figure, the left inset is a false-color electron micrograph of one of our multiprobe devices. The right inset is an atomic-force microscope image of a section of the nanowire of D1 with the color variation from black to white corresponding to a height variation of 16 nm. The lower-right inset is the result of an AFM line scan along the white dotted line shown in the AFM image in the upper-left quadrant of the figure. (b) Two-terminal transfer curves of D1, measured at various drain biases (indicated). Data for both sweep directions are included, with lighter/darker color corresponding to sweeping drain voltage down/up. The inset shows the data for V_d = 1.0 V with the current on a logarithmic scale. (c) Comparison of two- and four-terminal measurements of the transfer curve of D1. To allow comparison of these data, the measured resistances from the two measurements are converted into a resistivity. The variation of the transfer curve is also indicated for reference. The inset is a schematic of the TiS_3 crystal structure, with Ti/S atoms in black/yellow. The quasi-1D TiS_3 chains are assembled into 2D layers, which then stack into a three-dimensional structure. One of the chains is shown separately from two different perspectives to illustrate the quasi-1D nature of TiS_3 crystals.

chains (see the inset of Figure 1(c)). The chains are bound together in 2D sheets, coupled to one another by weaker van-der-Waals-like bonding.[12−16] Narrow TiS_3 whiskers could be grown through a direct reaction between metallic titanium and sulfur at 550 °C and then easily exfoliated into ribbons of nanoscale cross section. With lengths that often extend over distances of many micrometers,[17−20] these exfoliated TiS_3 nanowires are excellently suited to FET implementation.

The physical properties of TiS_3 have been studied in bulk for many decades.[22−34] From these works it is known that bulk TiS_3 is an indirect semiconductor, with an associated bandgap of around 1 eV. In temperature-dependent studies of its electrical properties, large crystals have been shown to undergo a metal−insulator transition (MIT), at a transition temperature (T_c) close to 220 K.[27,28] At temperatures below this scale, the material has been suggested[27,28] to develop a Peierls distortion,[35] resulting in the formation of a charge-density wave (CDW). The electrical properties moreover reflect the quasi-one-dimensional (1D) crystal structure, with the mobility being expected to depend upon the direction of current flow relative to the one-dimensional atomic chains.[17,20] Indeed, one study[15] has predicted a mobility as large as 10^4 $cm^2/(V\ s)$ along the (b direction of the) chains, more than an order of magnitude higher than that perpendicular to them. However, for reasons that have remained unclear, room-temperature reports of transport[17,18,20,30] and transient absorption[21] have consistently yielded much lower mobilities (10−50 $cm^2/(V\ s)$). Such discrepancies highlight the need for a comprehensive evaluation of the electrical characteristics of TiS_3, undertaken for a wide range of temperatures and carrier concentrations. It is just such a study that we present in this Article.

RESULTS AND DISCUSSION

The TiS_3 crystals used in this study were grown at 550 °C in evacuated ampules containing titanium and sulfur[20] (see the Supporting Information). FET structures (Figure 1(a), upper-left inset) were prepared by first using an adhesive tape[16] to exfoliate the synthesized material onto SiO_2 substrates, following which electron-beam lithography was utilized to define multielectrode structures (for further details, see the Methods section). Quite generally, the exfoliation produces crystals of various length, width, and thickness (for further details, see the Supporting Information), from which nanoribbons with well-defined wire-like geometries were selected. Some key properties of the two most extensively studied devices (D1 and D2) are indicated in Table 1. It should be noted here that, when we refer to the length of the transistor channel, we imply the internal length measured between a particular pair of current or voltage probes (as indicated, for example, in the electron micrograph in Figure 1(a)). The width and thickness of the nanowires were determined from atomic-force microscopy, as demonstrated in the lower-right

Table 1. Details of the Device D1[a]

device	W (nm)	L_{2T} (μm)	L_{4T} (μm)	t (nm)	V_T (V)
D1	125	5.1	20.5	6.8	−30
D2	253	4.3		7.8	−120

[a] W: nanowire width. L_{2T}: two-terminal probe separation. L_{4T}: voltage probe separation in four-terminal measurements. t: nanowire thickness. V_T: FET threshold voltage at room temperature. Dimensions were determined by a combination of atomic-force and scanning-electron microscopy.

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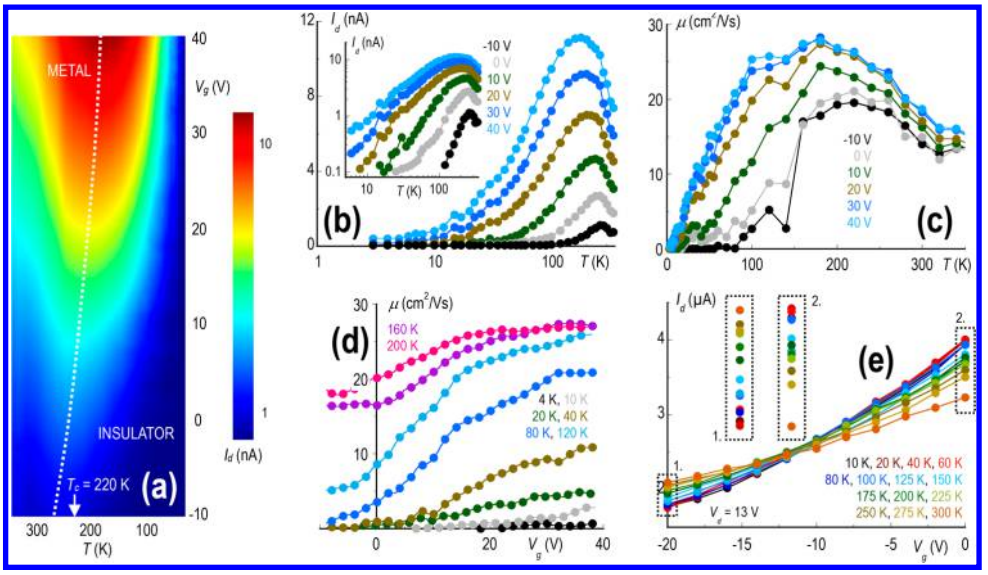

Figure 2. (a) Color contour indicating the variation of drain current as a function of gate voltage and temperature for D1. The white dotted line indicates the approximate boundary between the metallic and insulating states (current decreasing/increasing with increasing temperature, respectively). Data were obtained for a drain voltage V_d = 100 mV. (b) Variations of drain current with temperature for several fixed gate voltages (indicated) from (a). The inset shows the same data with current plotted on a logarithmic scale. (c) Variation of mobility with temperature, determined from the data of (b) (V_d = 100 mV) using the method of ref 42. (d) Variation of mobility with gate voltage, at various temperatures on the insulator side of the transition. (e) Transfer curves of device D1, measured at various temperatures and for V_d = 13 V. A fixed point indicative of an MIT can be seen near V_g = −12 V. The two insets indicate the variation of the current with temperature at the two ends of the transfer curve. Region 1/2 corresponds to insulating/metallic behavior.

inset of Figure 1(a). The transistor (drain current, I_d, *vs* drain voltage, V_d) and transfer (I_d *vs* gate voltage, V_g) curves of these devices were measured over a wide temperature range (3−450 K), encompassing that of the observed MIT.

In Figure 1, we present a number of representative results that illustrate the room-temperature operation of our devices. In the main panel of Figure 1(a), we show transistor curves for various gate voltages above threshold. Linear behavior is clearly observed around zero bias (a point that we return to below), while evidence for saturation is apparent at positive voltages. It will be apparent from the threshold voltages indicated in Table 1, and from the various curves of Figure 1(a), that the TiS_3 nanowire FETs are normally on devices, implying the n-type character of the material. In Figure 1(b) and (c), we plot transfer curves obtained under various conditions. In the main panel of Figure 1(b), we show transfer curves for both sweep directions and for different values of the drain bias. The normally on nature of the FETs is apparent in these plots, also, along with hysteresis that depends systematically on the sweep direction. Such hysteresis is well known[36−41] for TMD FETs formed on SiO_2 substrates and is usually attributed to the charging of interfacial states and of deep traps in the oxide layer. From the perspective of the study of interest here, the important point to note will be that the hysteresis always evolves systematically, with the value of the current being higher/lower when sweeping up to/down from large positive voltage. The nature of the hysteresis is moreover indicated in the inset to Figure 1(b), which plots the variation of the drain current on a logarithmic scale. Here it can be seen that the ON/OFF ratio for the device is around 10^2−10,[3] significantly lower than typically found for 2D TMD-based FETs;[4,5] this may largely be attributed to the nanowire geometry of our devices, which limits the absolute current carrying capacity in the ON state (to <10 μA, as opposed to ∼mA for typical 2D FETs).

While the results of Figure 1(a) and (b) were obtained in a typical, two-probe transistor geometry, in Figure 1(c) we illustrate the influence of contact resistance in the devices, by comparing the results of two- and four-probe transfer-curve measurements. To account for the different probe separations in the two measurements, the current variations obtained from them are converted into resistivities, which are compared directly in the figure. For the purpose of comparison, the variation of current obtained in the four-terminal measurement is also indicated in the figure. Inspection of the resulting variations shows that, within experimental uncertainty, there is no significant difference between the two- and four-terminal resistance, at least as long as the FET remains in its ON state. In other words, the measured resistance under such conditions should be dominated by the intrinsic resistance of the nanowire, with a much smaller contribution from any contact resistance. To further explore this issue, we have performed an activation analysis for the temperature-dependent I_d−V_d characteristics of these devices. While full details are given in the Supporting Information, the essential conclusion is that these devices are characterized by a small Schottky barrier (∼meV) at their contacts, a result that is consistent with the observations in Figure 1(c).

In the various panels of Figure 2, we present results of an electrical characterization of the nanowire FETs, obtained over a wide temperature range. The color contour of Figure 2(a) was compiled from measurements of the transfer curve, collected over the temperature range from 3 to 350 K. For further insight into the variations apparent in this contour, in Figure 2(b) we plot the temperature-dependent variation of the drain current from this contour, at a series of equidistantly spaced gate voltages (the various panels and the inset plot the same data on different scales). It is clear from these different figures that I_d varies nonmonotonically with temperature, initially increasing as the temperature is raised from 3 K (*i.e.*,

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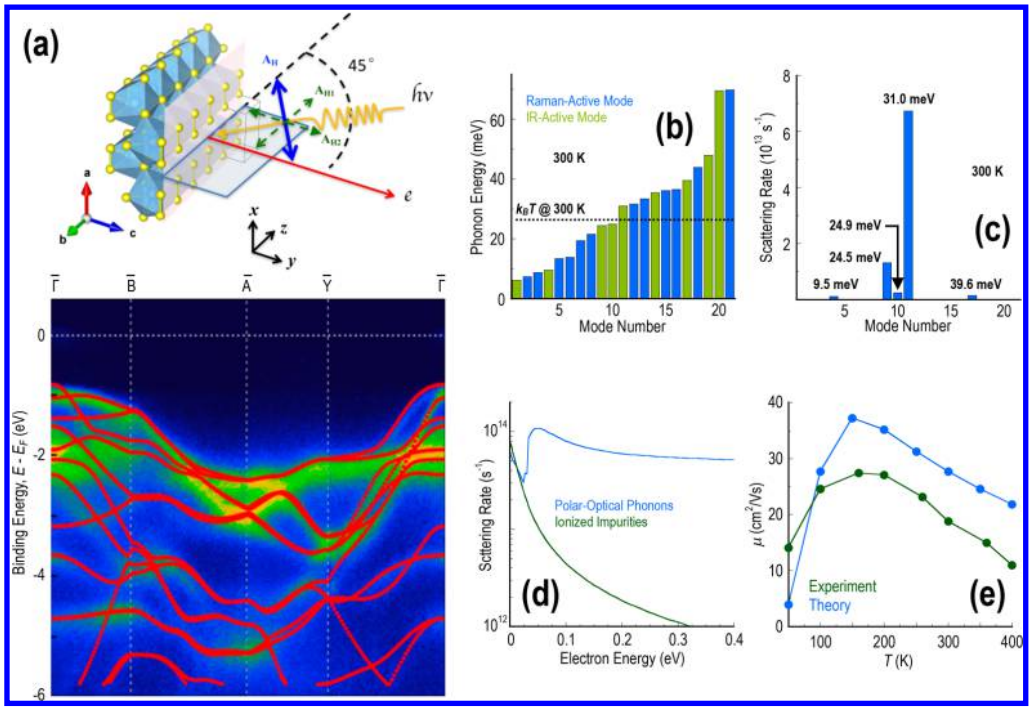

Figure 3. (a) Comparison of calculated valence-band structure with ARPES measurements of TiS_3 crystals. The upper panel is a schematic that shows the configuration of the ARPES measurements relative to the crystal structure. For further details on the ARPES study, as well as the band structure calculations, we refer the reader to the Supporting Information. (b) Calculated phonon modes for bulk TiS_3, along with their optical character (Raman- *vs* IR-active). (c) Calculated scattering rate of the different phonon modes for an electron with energy of 40 meV. The POP modes near 31 and 25 meV are dominant. (d) Calculated energy dependence of the scattering rate due to all 12 polar-optical phonon (POP) modes and ionized impurities. (e) Comparison of the experimental (D1, V_d = 100 mV) and calculated mobilities and their dependences on temperature.

an insulator-like variation), then peaking at some characteristic temperature. Beyond this point, the current decreases with further increase of temperature, a variation that is metal-like in nature. Roughly speaking, the crossover between the metallic and insulating regimes occurs close to 220 K, the established[27,28] critical temperature for the MIT in bulk TiS_3. More careful inspection, however, reveals this crossover to be density dependent, evolving (see the dotted line in Figure 2(a)) from ∼270 K to ∼180 K as the gate voltage (and so the carrier concentration) is reduced from +40 V to −10 V.

In Figure 2(c), we plot the variation of mobility as a function of temperature and gate voltage, inferred from the transfer-curve data of Figure 2(a) and (b). Mobility is calculated here using the approach described in ref 42. This method allows the mobility to be determined under conditions where it is gate-voltage dependent and yields the different curves plotted in Figure 2(c). According to these curves, the mobility is characterized by a general variation in which it increases first with increasing temperature, as expected in the insulating regime, before peaking at a temperature close to the bulk MIT T_c of 220 K, following which it decreases with further increase of temperature. The latter behavior is reminiscent of that exhibited by metals and semiconductors, in which phonon activation results in stronger carrier scattering as the temperature is increased.[43] In the low-temperature, insulating, regime, in contrast, the mobility is quenched as the temperature is lowered toward 0 K, reflecting the corresponding suppression of the drain current in this regime.

The variation of mobility as a function of gate voltage (proportional to carrier density) is plotted at various temperatures on the insulator side of the MIT in Figure 2(d). At the lowest temperatures (<100 K), these data are characterized by a strong increase of μ as the gate voltage is raised beyond threshold (a variation that corresponds to an approximately linear dependence), followed by a crossover to a much slower variation at larger gate voltages (V_g > ∼30 V). The 200 K data, on the other hand, lie close to the MIT and so consequently only exhibit a much slower dependence on gate voltage, consistent with the influence of incipient metallic conduction.

A characteristic feature of an MIT is the presence of a fixed point[44] in physical properties such as resistance, as a function of some suitable control parameter (*e.g.*, temperature or carrier concentration). An example of such a fixed point is demonstrated in Figure 2(d), in which we plot the transfer curve of one of the nanowire FETs, at a series of different temperatures. A crossing point is clearly apparent in these data (Figure 2(e)), with insulating behavior apparent for V_g < −12 V and metallic behavior at larger voltages. The presence of this crossover suggests the existence of a true MIT in this system, the occurrence of which may be manipulated *via* the carrier concentration. When this concentration is sufficiently low (V_g < −12 V in Figure 2(e)), the system remains insulating over the full temperature range studied. By increasing the electron concentration *via* the gate voltage, however, a transition to metallic behavior is seen. This concentration dependence of the metal−insulator crossover is an important aspect of this work, which was absent from studies of bulk crystals,[27,28] in which electrical gating of the material was not utilized.

In a recent theoretical study[15] of the transport properties of TiS_3, room-temperature mobility as high as 10^4 $cm^2/(V\,s)$ was predicted along the direction of its one-dimensional Ti chains

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(*i.e.*, along the *b*-axis that corresponds to the long direction of the nanoribbons studied here). The data of Figure 2(c) are some 2−3 orders of magnitude smaller than this, however, a huge discrepancy that requires clarification. In order to provide this, we have carried out comprehensive calculations of transport in the nanowires, using *ab initio* methods to account for the details of the electron−phonon interaction. While the essential features of our model are described more comprehensively in the Supporting Information, the essential feature of our work is that it accounts for the influence of electron scattering by polar-optical phonons (POPs). While POP scattering is an important mechanism that limits mobilities in most polar semiconductors,[45−47] its influence was neglected in ref 15. In this work, however, we consider the contribution of this mechanism explicitly, computing the contribution of long-range interaction elements between electrons and POPs to the mobility.

The starting point for our analysis is a calculation of the electronic band structure of TiS_3 in Quantum Espresso (Supporting Information), which yields the valence band dispersions plotted in Figure 3(a). In this figure, we plot the curvature of the energy bands along the principal directions of the reciprocal lattice, superimposing them upon the valence band structure deduced from ARPES measurements[48] of bulk TiS_3. The agreement here is clearly impressive, giving us confidence in the veracity of the calculated electronic structure. To characterize the lattice response, we perform calculations based on density functional perturbation theory (DFPT). The eight-atom unit cell of TiS_3 yields 24 phonon modes, whose energies are indicated in Figure 3(b); nine of these modes are IR-active POPs, while 12 are nonpolar (*i.e.*, Raman) optical modes. The calculated Raman modes are in good agreement with experimental reports,[49−51] and, at room temperature, modes 12 (24.51 meV), 13 (24.93 meV), and 14 (31.02 meV) are expected to contribute most strongly to electron scattering, as they have high IR strengths (Figure 3(c)). In Figure 3(d), we show the energy-dependent scattering rate calculated for POPs, showing that the strong contributions from the aforementioned three modes yield a fairly constant scattering rate over a wide range of electron energy. For comparison, the figure also includes the corresponding rate for ionized-impurity scattering[52] (see Supporting Information). For this latter mechanism, we have taken advantage of prior studies of bulk conduction in TiS_3, which have shown it to be an unintentionally doped n-type conductor (consistent with our transfer curves in Figures 1 and 2), with a dopant activation energy of 80 meV.[28,30] The dopant concentration (7×10^{18} cm^{-3}) used in these calculations was determined by forcing the calculated transfer curves to match the experimental ones (see Supporting Information). The results obtained in Figure 3(d) confirm that POP scattering, rather than scattering from ionized impurities, will dominate the mobility, and it is this fact that is responsible for the discrepancy between the very large mobilities calculated in ref 15 and those observed in the experiment here (and in prior work[30] on bulk crystals). In Figure 3(e), we compare the temperature dependence of the electron mobility, determined from experiment and from calculations that include the influence of both mechanisms from Figure 3(d). The agreement between experiment and theory is good, in terms of both overall trend (*i.e.*, nonmonotonicity) and the crossover temperature (~200 K) between the insulating and metallic behaviors. There is some difference (~50%) in the magnitude of the observed and calculated mobilities, but this is considered reasonable given the uncertainty regarding the detailed microscopic structure of the nanowires and the fact that the influence of the SiO_2 substrate on conduction is not addressed here.

The analysis of Figure 3 casts important light on the mobility variations found in experiment. First, it demonstrates that the large discrepancies between our observations and the much larger mobilities predicted in ref 15 arises from the failure to consider the influence of POP scattering in the latter work. Rather, the decrease of mobility with increasing temperature, apparent beyond 200 K in Figure 3(e), is attributed to an associated growth in the strength of POP scattering. At lower temperatures, in the insulating regime, the situation is more complicated, however. The computed mobility in Figure 3(e) shows a general decrease as the temperature is lowered that is reminiscent of that seen in the experiment. In these calculations, the decrease is attributed to the increased importance of ionized-dopant scattering, which can overwhelm phonon scattering at low temperatures.[43] In reality, however, we believe that the behavior observed in this limit should be attributed to an MIT, resulting in the formation of an insulating state as the temperature is lowered. In support of this, we note that the crossover to this insulator occurs in a temperature range associated with the MIT in bulk[27,28] TiS_3. In the literature, at least, the transition to the insulating state has been attributed to the formation of a CDW,[27,28] arising from a Peierls distortion[35] of the crystal lattice.

An interesting feature of transport in the insulating regime is the presence of mesoscopic conductance fluctuations, which are manifested in the transfer curves of Figure 4. The temperature dependence of these features is plotted in Figure 4(a), while their dependence on drain bias is indicated in the inset of Figure 4(b). As the temperature is increased from its lowest value, there is a gradual increase in the overall current, behavior that is accompanied by an increase in the absolute amplitude of the current fluctuations (see the curves in Figure 4(a)). In the main panel of Figure 4(b) we confirm the reproducibility of these features, plotting the results of three successive measurements of the transfer curve, under identical conditions at 20 K. Overall, the reproducibility is high, although it is clear that there is a smaller, fast component of the fluctuations that is not well reproduced. This component is most prominent in the measurements made at the lowest temperatures (see the 3 and 10 K curves in Figure 4(a)), where the current level is in the sub-nA range. In this limit, the fluctuations most likely arise from a combination of instrumentation noise and time-dependent instabilities in the conductance.

Mesoscopic fluctuations are well known from the study of dirty metal and semiconductors and are typically strongly damped with increasing temperature as electron coherence is suppressed.[53] The fluctuations in Figure 4 are quite different in nature, however, as we indicated in the inset to Figure 4(c). This shows that, with initial increase of the temperature from 3 K to 50 K, the (root-mean-square) amplitude of the current fluctuations (δI_{RMS}) grows rather than decreases. Having reached a local maximum at 50 K, the amplitude of fluctuation then decays, until becoming fully quenched at a temperature around 200 K.

There are several interesting aspects of the behavior highlighted above, the first of which is the nonmonotonic dependence of the fluctuation amplitude on temperature. Such behavior is not normally associated with mesoscopic

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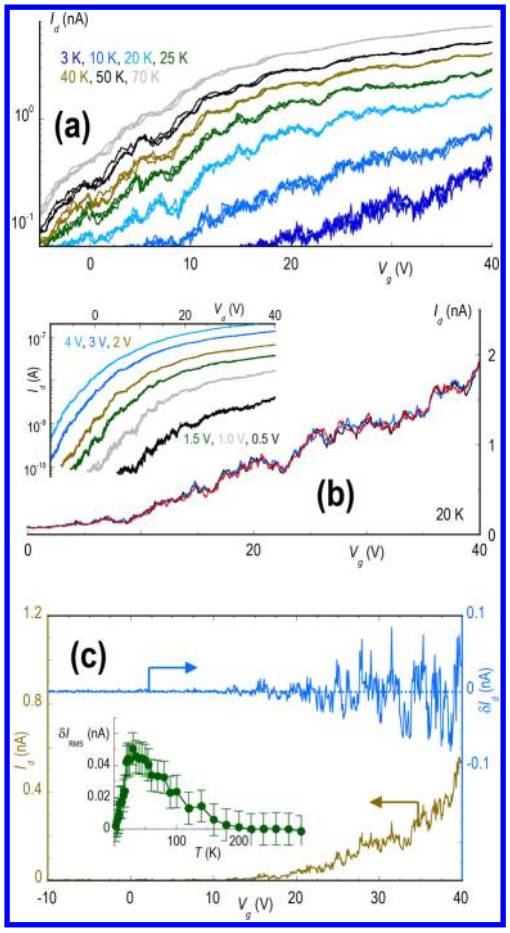

Figure 4. (a) Measured transfer curves of D1 from 3 to 70 K, indicating the presence of mesoscopic current fluctuations. At each gate voltage, the results of three successive measurements are plotted to indicate the reproducibility of this behavior (V_d = 1.0 V). (b) The reproducibility of the fluctuations is further indicated here, where we show results of three successive measurements of the transfer curve of D1 (20 K, V_d = 100 mV). The inset plots measured transfer curves of the same device at various values of V_d (indicated). (c) The main panel plots the transfer curve (green) of D1 at 3 K (V_d = 1.0 V) and the fluctuating component (δI_d, blue) of this current. The inset shows the temperature dependence of δI_{RMS}, the root-mean square current fluctuation measured over the gate voltage range from −10 to +40 V.

fluctuations,[53] but can be explained by considering the influence of the temperature on the overall conductance level. As can be seen in Figure 4(a), due to the insulating nature of the system below 220 K, increasing temperature leads to an increase in background conductance. As this occurs, there is actually a range of temperature for which the amplitude of the current fluctuations grows. This can be seen in the transfer curves of Figure 4(b) and (c), also, in which the fluctuating component of current clearly grows in concert with the overall current level. In Figure 4(c) we highlight this explicitly by comparing the fluctuating component of the current (δI_d, blue) to the transfer curve (brown).

The other unusual feature of the fluctuations described here is their persistence to high temperatures, very much higher than those reported previously. This is highlighted in the inset to Figure 4(c), which shows that it is only once the temperature is increased beyond ∼200 K that the fluctuations are fully suppressed (the error bars in this figure reflect the noise in the current noted earlier). Intriguingly, this temperature correlates closely to the transition temperature of the MIT (Figure 3), suggesting that the fluctuations are somehow inherently related to the insulating state. With this connection noted, the nonmonotonic temperature dependence of these features would appear to arise from a competition between the tendency for increasing temperature to initially enhance conduction in this state and for it to suppress quantum coherence in transport[53] at even higher temperatures.

The MIT in bulk TiS_3 has previously been connected to the possibility of CDW formation, a known signature of which is strong nonlinearity near zero bias in the current−voltage characteristic.[35] Evidence of such behavior is presented in Figure 5, in the main panel of which we show a measured set of

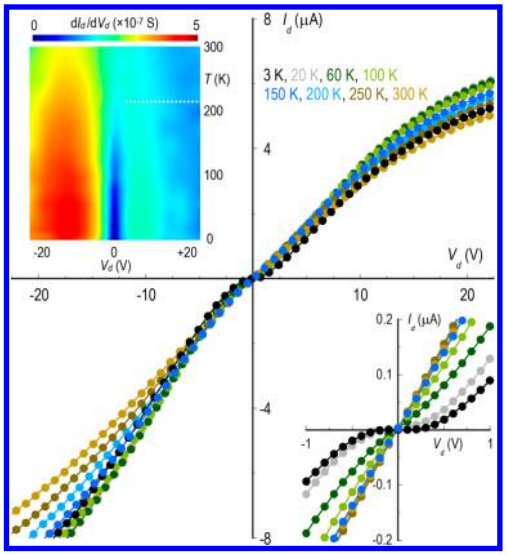

Figure 5. The main panel shows the results of two-terminal measurements of the transistor curves of D1 at various temperatures (V_g = 0 V). The lower-right inset is an expanded view around the origin of the main panel, indicating a strong nonlinearity in current near zero bias. The upper-left inset plots the variation of differential conductance as a function of temperature, determined from data such as those shown in the main panel. The deep-blue coloring near zero bias indicates a suppression of conductance at low temperatures, which washes out as the temperature of the MIT (white dotted line) is approached.

transistor curves at various temperatures from 3 to 300 K. The lower-right inset is an expanded view of these curves, illustrating more clearly the strong suppression of the current near zero bias and at low temperatures. While nonlinearity similar to that shown in this inset is widely observed in nanoscale FETs, it is typically understood to arise from nonohmic injection *via* tunneling contacts.[53] Such an effect can be excluded here, where the nonlinearity instead appears to be an intrinsic feature of the nanowires; although the data of Figure 5 were obtained in a two-probe configuration, as appropriate for normal transistor studies, we have also performed four-probe measurements of the transistor curves (see Supporting Information) and find that these, too, exhibit the same suppression of current near zero bias. Since such measurements eliminate the influence of contact resistance, CDW formation seems a plausible origin for the observed nonlinearity. In the upper-left inset of Figure 5, we plot the differential conductance calculated (by numerical differ-

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entiation) from transistor curves such as those shown in the main panel. The figure reveals a strong suppression of the zero-bias conductance at low temperatures, as expected from the data in the main panel. This suppression is clearly overwhelmed with an increase of temperature, with the contour plot revealing that it is no longer observed once the temperature is increased beyond ∼220 K. Obviously, this agrees well with the critical temperature of the MIT and supports the notion that the low-bias nonlinearity in the transistor curves could indeed be a signature of a CDW insulator.

Previously, there have been several reports of CDW formation in bulk crystals of both TMDs[54,55] and TMTs.[28−33] More recently, there have even been reports of MITs and of CDW formation in the two-dimensional counterparts of these materials, most notably in the TMDs.[56−59] With regard to TMTs, recent work[60] has provided evidence for CDW formation in TiS_3 nanoribbons, similar to those studied here. In the study of ref 60, the authors provided evidence of additional transition temperatures for this system, separate from that of the MIT, and suggested that these were related to the properties of the CDW. No such features were found in this study, however, and we consider that a more definitive demonstration of CDW formation is called for. Indeed, in separate photoemission studies[48] of bulk (ungated) TiS_3 crystals, we have not observed any signatures of CDW formation. It is possible that this discrepancy with the results here arises from the fact that we are able to gate the nanowires, to induce the free conduction required to support CDW formation. A further possibility that cannot be excluded is that the observed MIT instead reflects the presence of some defect-mediated impurity band, which freezes out at low temperatures. To resolve these possibilities, a more definitive identification of the density-wave state is required, such as the well-known current-oscillation phenomenon that can be generated by simultaneously applying AC and DC electric fields to the CDW.[35] While such a study lies beyond the scope of the present work, it should be undertaken in the future.

CONCLUSIONS

In conclusion, we have undertaken a wide-range (3−350 K) characterization of the electrical characteristics of TiS_3 nanowire FETs. These nanomaterials are characterized by a quasi-one-dimensional metal-chain structure, which is expected to render them amenable to CDW formation. The temperature-dependent transfer curves of these devices show evidence for an MIT, with a crossover temperature (∼220 K) in accordance with prior observations for bulk material. In contrast to bulk TiS_3, but in accordance with observations for 2D TMDs,[57] the transition exhibits a gate-controlled character, as indicated by the presence of a fixed point in the transfer curves. The room-temperature mobility of these devices (∼20−30 $cm^2/(V\ s)$) was found to be some 2−3 orders of magnitude smaller than theoretical predictions[15] for this system, a result that we explained by including the influence of POP scattering in calculations of the transport. With the influence of this mechanism accounted for, the computed variation of mobility as a function of temperature was found to show good quantitative agreement with experiment. This included the overall magnitude of the mobility and the nonmonotonicity associated with the crossover from the metallic to the insulating state. In the insulating state, below ∼220 K, the transfer curves exhibit unusual mesoscopic fluctuations and a suppression of the current near zero bias that is common to CDWs. The fluctuations have an anomalous temperature dependence, finally washing out at a temperature close to that of the MIT, suggesting that they may somehow be a feature of quantum interference in the insulating (CDW) state. Overall, our results demonstrate that quasi-1D TiS_3 nanostructures represent a viable candidate for FET realization and that the functionality of these devices can be influenced by complex condensed-matter phenomena.

METHODS/EXPERIMENTAL

The TiS_3 crystals used in this study were mechanically exfoliated onto Si/SiO_2 substrates, yielding TiS_3 nanoribbons with thicknesses down to a few nanometers. Having identified these ribbons by optical microscopy, and after confirming their structure in an atomic-force microscope, electron-beam lithography was used to prepare the multielectrode FETs. We have previously found[16] that Raman spectroscopy may only be used to differentiate between TiS_3 crystals whose thickness ranges from one to about seven monolayers. Considering that the interlayer distance in the TiS_3 structure is about 0.9 nm, the nanowires used in devices D1 and D2 were therefore sufficiently thick (6.8 and 7.8 nm, respectively) to exhibit Raman spectra characteristic of bulk material (for an example of the bulk Raman spectrum of TiS3, see Figure S2(d)). The thickness of the SiO_2 was 300 nm, and the conducting (p-type) Si substrate served as a back-gate in the measurements. The Cr/Au electrodes were formed by a combination of electron-beam lithography and lift off, with thicknesses of 3 and 20 nm, respectively. As shown in the upper-left inset to Figure 1(a), the nanowires were around 100 nm wide and were of uniform width over many micrometers. Inspection by atomic force microscope revealed a typical thickness of a few nanometers, ranging from 2 to 10 nm, dependent upon the device. Five different devices were measured for this study, and all showed quantitatively similar behavior. For illustrative purposes, we present here the results of a detailed study of one of these devices (labeled D1), although similar results were also obtained in a detailed study of a second device (D2). (Additionally, the operational characteristics of the nanowire FETs have been reproduced in room-temperature measurements of several more devices.) Samples were mounted in a ceramic DIP package and installed in the vacuum space of a cryogen-free cryostat. This system allowed electrical properties to be measured over a wide temperature range (3−450 K), under vacuum conditions. Transistor (I_d *vs* V_d) and transfer (I_d *vs* V_g) curves were measured in this setup, using either a Keithley 2400 SMU (source-measure unit) or a 6517A electrometer. The multiprobe geometry of the nanowire FETs allowed their channel to be probed in both two- and four-terminal configuration, thereby allowing us to identify the contribution of the contacts to the total resistance.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b08260.

Additional information on the nanowire synthesis and structural characterization, theoretical calculations, and the ARPES and electrical measurements (PDF)

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Notes

The authors declare no competing financial interest.

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