“Energy efficient computing for the sub-14nm era: challenges and opportunities”

Abstract: This lecture presents some of the prominent barriers to designing energy-efficient circuits in the sub-14nm CMOS technology regime and outlines new paradigm shifts necessary in next-generation multi-core microprocessors and systems-on-chip. Emerging trends and key challenges in sub-14nm design are outlined, including (i) device and on-chip interconnect technology projections, (ii) performance, leakage and voltage scalability, (iii) special-purpose hardware accelerators and reconfigurable co-processors for compute-intensive signal processing algorithms, (iv) fine-grain power management with integrated voltage regulators, and (v) resilient circuit design to enable robust variation-tolerant operation. Energy-efficient arithmetic and logic circuit techniques, static/dynamic supply scaling, on-die interconnect fabric circuits, ultra-low-voltage and near-threshold logic and memory circuit techniques, and multi-supply/multi-clock domain design for switching and leakage energy reduction are described. Special purpose hardware accelerators and data-path building blocks for enabling high GOPS/Watt on specialized DSP tasks such as encryption, graphics and media processing are presented. Power efficient optimization of microprocessors to span a wide operating range across high performance servers to ultra mobile SoCs, dynamic on-the-fly configurability and adaptation, and circuit techniques for active/standby-mode leakage reduction with robust low-voltage operability are reviewed. Specific chip design examples and case studies supported by silicon measurements and trade-offs will be discussed.

Bio: Ram Krishnamurthy received the B.E. degree in electrical engineering from Regional Engineering College, Trichy, India, in 1993, M.S. degree in electrical and computer engineering from State University of New York at Buffalo in 1995, and Ph.D. degree in electrical and computer engineering from Carnegie Mellon University in 1998. He has been with Intel Corporation since 1998, where he is Senior Principal Engineer and heads the high performance and low voltage circuits group at Circuits Research Labs, Intel Labs, Hillsboro, Oregon. He is responsible for research in high performance, energy efficient and low voltage circuits for microprocessors and SoCs. He holds 100 issued patents with over 50 patents pending and has published 150 conference/journal papers and 3 book chapters on high-performance energy-efficient microprocessor design. He serves as Intel's representative on the Semiconductor Research Corporation technical advisory board for circuits. He has served as associate editor of IEEE transactions on VLSI systems, guest editor of IEEE journal of solid-state circuits and on the technical program committees of ISSCC, CICC, and SOCC conferences. He served as Technical Program Chair/General Chair for the 2005/2006 IEEE International Systems-on-Chip Conference and presently serves on the conference's steering committee. He serves as ECE department adjunct faculty at Oregon State University, where he taught advanced VLSI design. He also serves on industrial advisory board of Oregon State University and State University of New York at Buffalo EE departments. He is a Fellow of the IEEE and distinguished lecturer of IEEE solid-state circuits society.